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STANDARD AVIONIC MODULE STUDY.(U)
MAR 78 D B MCBRAYER, G R COURTNEY, A R TOMME N00123-77-C-0094
UNCLASSIFIED NL

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Naval Weapons Center

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A. R. Tomme

(12) 183p.

VOUGHT CORPORATION
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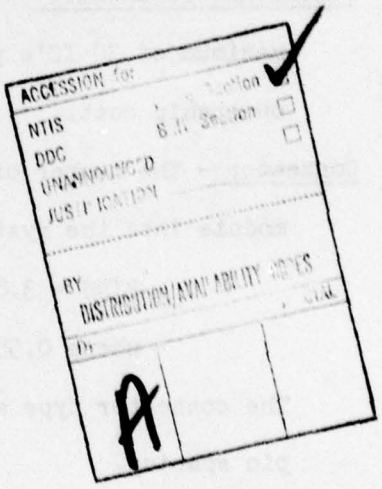
FOREWORD

This report was prepared by Vought Corporation, under Naval Weapons Center Contract N00123-77-C-0094, Work Assignment 0008. The program was administered and monitored by Mr. James McGuire of NWC. This document is the final report for the program which initiated 11 October 1977 and continued through 1 March 1978.

The Principal Investigator for this program was Mr. D. B. McBrayer and the Technical Project Engineer was Mr. R. K. Mahaffey. Principal contributors to the research and report were Mr. G. R. Courtney and Mr. A. R. Tomme.



SUMMARY

This report covers the Standard Avionic Module (SAM) study performed by Vought Corporation under Contract N00123-77-C-0094, Work Assignment 0008 for the Naval Weapons Center. The purpose of this study was to propose the characteristics of a standard module based upon the data and conclusions of previous Navy studies. The proposed module should satisfy the greatest majority of requirements enumerated in the final reports for those studies.

The data base and reference reports were reviewed to determine those factors which significantly affect the selected size of a standard module. Each of these factors were analyzed based upon a compilation of data from the reports and conclusions reached on each individual factor. These factors and the conclusion reached in each area are summarized as follows:

Functional Commonality:- The packaging concept should provide for a maximum of 30 IC's per module to achieve any savings in total ownership cost.

Connector:- The number of pins required to electrically interface the module into the system can be estimated by the relationship;

$$PINS = 3.8\ G^{r},$$

where $0.58 > r > 0.52$

The connector type should be the NAFI blade and fork with 0.1 inch pin spacing.

Integrated Circuit Packaging Technology:- Present technology is 14-16 pin IC with an average of approximately 18 gates per IC. The 1985 technology is projected to be a 40 pin IC with an average of approximately 100 gates per IC. The dual-in-line package will be more widely used than flatpacks. The chip carrier package can provide a higher gate density package.

Weight and Volume Constraints - The module active area should be greater than 10 square inches (more than 20 dual-in-line IC's) to minimize effect of overhead volume.

Thermal Considerations - Thermal conduction requirements can be satisfied within size limitations set by IC count using DIP packaging.

Built-In-Test - The inclusion of BIT increases the complexity and size of a system by 15 to 25%.

Reliability - The module should contain 27 or less 14-16 pin IC's using TTL logic with maximum junction temperatures of 105°C. With junction temperatures of 85°C, the maximum number of 14-16 pin IC's can be increased to 30.

These individual conclusions do not clearly indicate the exact number of integrated circuits which should be contained on a standard module. However, a range of optimum integrated circuit component capability of between 20 and 30 is indicated. This information along with a compilation of the number of integrated circuits required for several recommended standard functions resulted in the choice of 30 integrated circuits for the standard module.

Using 30-16 pin dual-in-line packages and a 100 pin interface connector, a 4.0 inch by 6.0 inch module was derived which can provide the desired thermal and vibration characteristics. This module was compared with other modules described in the Data Base reports and was found to be near the mean value of area, height, width and aspect ratio of the previously proposed modules. A list of 44 potential standard or common functions compatible with the proposed module size and taken from the Data Base Reports has been prepared and is provided.

In the process of performing this study, several areas of concern in the establishment, implementation and maintenance of a successful standard avionic module program were identified. Resolution of these items should be accomplished

prior to the initiation of the specification or design of module hardware. These items and a recommended method for each of obtaining a satisfactory resolution are as follows:

(a) EMI/EMP - A thorough analysis of the entire system requirements for providing satisfactory protection against the effects of EMI/EMP/EMV should be accomplished to establish the attenuation budget for each level of avionic packaging such as aircraft skin, rack enclosure, and individual modules. In addition, the required interface restrictions for electromagnetic radiation, susceptibility and conduction should be established. It is recommended that a program be initiated to: (1) establish the design requirements, (2) design, construct and test a typical system and (3) prepare the applicable EMI specification.

(b) MAINTENANCE PHILOSOPHY - The maintenance philosophy to be used for programs using the standard modules should be established prior to the preparation of the functional specification for the individual modules. It is recommended that a program be initiated to establish an overall avionic system maintenance philosophy and to prepare detail specifications for the individual subsystems and individual modules.

(c) ENVIRONMENTAL - The effects of vibration, humidity and salt-sea atmosphere on the SAM design concept should be evaluated. It is recommended that a test program be initiated to perform environmental tests on a typical subsystem mounted in an avionic rack. This program can be used to evaluate various design concepts for the modules as well as the total rack installation.

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1.0 INTRODUCTION

This final report documents the results of a study to establish a proposed Standard Avionics Module (SAM) in conformance with the requirements of Work Assignment 0008 of Contract N00123-77-C-0094.

The purpose of the study is to postulate standard module characteristics which provide high applicability to multiple avionic equipments based upon information and data provided in 14 previous reports prepared by various companies and government organizations. These reports are divided into two major groups: (1) Data Base, consisting of 8 reports prepared under Navy contracts or by Navy organizations and primarily containing evaluations of Standard Electronic Modules (SEM) applications for avionic systems and (2) Reference Material, consisting of 6 reports and instructions covering various subjects related to the standard module concept. These reports are listed in Tables 1-1 and 1-2 for reference. The footnote references herein refer to the corresponding numbers in the bibliography. The study was conducted in three primary phases. These were:

(1) Analyze, compile, and summarize data from Data Base and Reference Material.

(2) Determine and describe module physical characteristics.

(3) Compare postulated module characteristics and capabilities with modules described in Data Base reports.

The results of each phase of the study are presented, along with all substantiating data, in the following paragraphs.

Table 1-1

DATA BASE REPORTS

- NADC REPORT - "Standard Electronic Module Program, Status Report", May 1976
- HONEYWELL REPORT - "Feasibility Study - Standard Modules for Avionics", June 1976
- NAFI REPORT TR 2146 - "Standard Electronic Modules, FY 1976 Summary Report", Sept 1976
- HONEYWELL REPORT - "Evaluation of Improved Standard Electronic Modules (ISEM) for Avionics", Oct 1976
- RAYTHEON REPORT - "Evaluation of Integrated Electronic Warfare System Circuit Functions for Standard Electronic Modules (SEM)", Feb 1977
- NAFI REPORT TR 2173 - "Standard Electronic Modules, An Evaluation of Three Module Sizes for Potential Standardization", March 1977
- GENERAL ELECTRIC REPORT - "Standard Electronic Module (SEM) Applications in Advanced Integrated Display Systems (AIDS) Program", May 1977
- TELEPHONICS REPORT - "Standard Electronic Module (SEM) Study of General Purpose Multiplex System (GPMS)", Preliminary Dec 1977

Table 1-2

REFERENCE MATERIAL

- IBM REPORT - "Advanced Standard Electronic Module (SEM) Packaging Trade Off Study" (November 1975)
- WESTINGHOUSE REPORT - "Modular Packaging Approaches" (June 1976)
- DEFENSE MATERIEL SPECIFICATIONS AND STANDARDS BOARD REPORT - "Standard Modules Subpanel to the Electronics Panel Final Report" (August 1976)
- EG&G REPORT - "Air Force/Industry Standard Electronic Module Workshops" (Sept 1976)
- NAVMAT INSTRUCTION 3960.9 - "Built-In-Test (BIT) Design Guide" (Sept 1976)
- HUGHES REPORT - "Function and Configuration Analysis Program" (October 1976)

2.0 DATA BASE DESCRIPTION

The Data Base and Reference material used during this study consists of reports and instructions prepared and accumulated during prior study efforts. These documents are tabulated in Tables 1-1 and 1-2. Each report is summarized in the following paragraphs for reference purposes.

2.1 Data Base Reports

2.1.1 NADC Report, "Standard Electronic Module Program, Status Report", May 1976 - This report is the Final Report on ATR Packaging for the Navy Standard Electronic Module (SEM) R&D Program. The purpose of this study was to determine the most efficient packaging enclosure for SEM. The conclusions reached in this study indicate that compatibility with ATR cases can be achieved by selecting one of 6 approximate module sizes. These 6 sizes are:

Designation	Height	Width
A1	2.75	2.687
B1	2.75	4.0
D1	2.75	6.625
D2	4	6.625
D4	6.5	6.625
F4	6.5	9.25

It is also recommended that the ARINC 3/8, $\frac{1}{2}$ and 3/4 Short ATR cases, as well as a short 1 ATR case (non-ARINC) be adapted as the standard higher level packaging for Standard Electronic Modules.

2.1.2 Honeywell Report, "Feasibility Study - Standard Modules for Avionics", June 1976 - This report presents the results of a study to define Standard Electronics Modules (SEM) which would reduce the life cycle cost of Navy avionics

systems. A single module size of 6" x 4" is recommended for use as the SEM. Information is also provided for functional partitioning of three avionic systems, the Visual Target Acquisition Set (VTAS), Laser Inertial Navigation System (LINS) and the A-7 Digital Flight Control System (DFCS), into the SEM. Eleven recommended SEM functions are defined.

2.1.3 NAFI Report, "Standard Electronic Modules, FY 1976 Summary Report", September 1976 - This report summarizes the module packaging studies accomplished jointly by NAFI and NWSC. The study concluded that the improved Standard Electronic Modules (SEM) family is the optimum selection for a new module family based upon functional data base analysis, trade-off criteria analysis, cost bounds analysis and the desireability of retaining packaging compatibility with the existing SEM program. The functional analysis indicated that a module with approximately 14 square inches of active component mounting area and 100 input/output connector pins will satisfy 95 percent of the standard functions, using dual-in-line packages, included in the study.

The report contains data on current and projected microelectronic device packaging technology and information on specific device sizes for use in determining the impact of the different device packages on the standard module size.

2.1.4 Honeywell Report, "Evaluation of Improved Standard Electronic Modules (ISEM) for Avionics", October 1976 - This report presents the results of a follow-on to a previous Honeywell study (see "Feasibility Study - Standard Modules for Avionics", paragraph 2.1.2 herein). The follow-on study evaluated the Improved Standard Electronic Module (ISEM) to determine the feasibility and desirability of using the ISEM 2A module to implement the three avionic systems considered in the earlier study. This study concluded that a 6 inch by 4 inch SEM is superior

to the ISEM 2A module for most criteria of comparison. This report provides information on the partitioning of the three avionic systems addressed in the original study into functions and circuits compatible with the ISEM 2A size. An evaluation of the AN/UYK-30 microprocessor capability to meet the necessary operational requirements of systems with high speed data processing is also provided.

2.1.5 Raytheon Report, "Evaluation of Integrated Electronic Warfare System Circuit Functions for Standard Electronic Modules (SEM)", February 1977 - This report presents the evaluations and recommendations for packaging of future Electronic Warfare (EW) circuits using Standard Electronic Modules. Ten circuit functions were selected as candidates for SEM packaging with detailed analysis being conducted on three of these functions. These three functions were separated into six SEM with the general electrical and interface requirements determined and cost estimates presented for each module. Preliminary specification sheets are presented for two of the selected SEM candidates.

2.1.6 NAFI Report, "Standard Electronic Modules, An Evaluation of Three Module Sizes for Potential Standardization", March 1977 - This report presents the results of an evaluation of five module configurations for packaging of the Modular Digital Scan Converter (MDSC) display system developed by Hughes Aircraft Corp. (HAC) for the Air Force. The five configurations included three proposed standard module configurations, the original HAC configuration and the existing SEM type 1A module. The study concluded that the improved SEM package yielded the least system weight and volume and provided the highest potential inter-system functional commonality (66%).

2.1.7 General Electric Report, "Standard Electronic Module (SEM) Applications in Advanced Integrated Display Systems (AIDS) Program", May 1977 - This report summarizes the results of a study to investigate the use of the SEM in packaging the Advanced Integrated Display System (AIDS). Four modules were selected and a preliminary design of each is provided including mechanical layouts using a module 4.55 inches in height and 6.75 inches in width.

2.1.8 Telephonics Report, "Standard Electronic Module (SEM) Study of General Purpose Multiplex System (GPMS)", Advance Copy - December 1977 - This report presents the results of a study to define optimum SEM designs of the General Purpose Multiplex System (GPMS). The GPMS has been partitioned into 3 unique SEMs.

2.2 Reference Reports

2.2.1 IBM Report, "Advanced Standard Electronic Module (SEM) Packaging Trade-Off Study", November 1975 - This report presents the results of a packaging technology trade-off study which compared the existing SEM configuration with other computer/processor configurations. The packaging technologies considered were SEM 1A. SEM 2A, NELC QED, IBM ML-1 Page and a modified ML-1 Page. The conclusions reached during this study were:

(a) Dual-in-line packages will be more widely used than flatpacks

(b) The ML-1 page produces the more efficient package from a volumetric standpoint

(c) The SEM 2A module offers a cost advantage for dual-in-line packaging. The modified ML-1 page and the SEM 2A are both cost effective for flatpack packaging.

2.2.2 Westinghouse Report - "Modular Packaging Approaches", June 1976 - This program performed studies to investigate the feasibility, practicality and implementation of standard electronic modules (SEM) for avionics. The studies included an analysis of past and present module programs, an analysis of present technology and its trend relative to a standard module concept and the compilation of data concerning standardization. Several conclusions are presented with the primary ones being:

(a) Functional partitioning by basic mathematical functions shows promise as an approach for defining SEM candidate circuits.

(b) Avionics environmental requirements do not pose a significant problem for SEM design.

(c) Major physical limitation for SEM will be I/O pin limitations and component configuration.

(d) The ATR is recommended for the LRU configuration. Standard module sizes can be established to fit the recommended ATR size.

(e) Acquisition cost is the major part of the life cycle cost for a system using SEM. The cost of spares is the major part of the logistic support cost.

2.2.3 Defense Materiel Specifications and Standards Board Report, "Standard Modules Subpanel to the Electronics Panel Final Report", August 1976 - The Standard Modules Subpanel examined the merits, means and long range implications of the widespread use of Standard Electronic Modules (SEM) and examined the interrelationship between microelectronic devices and the concept of standard electronic modules. This report summarizes the results of several other programs.

2.2.4 EG & G Report, "Air Force/Industry Standard Electronic Module Workshops", September 1976 - This report summarizes the information gathered during several workshops on standard electronic modules (SEM) which were held with key individuals in industry and the military to investigate the technical and economic feasibility of using SEM in proposed and existing Air Force systems. The report includes data and information in the areas of functional partitioning, mechanical/environmental interfaces, impact of technologies and maintenance concepts.

2.2.5 NAVMATINST 3960.9, "Built-In-Test (BIT) Design Guide", September 1976 - This guide provides information covering the aspects of built-in-test (BIT) at all levels of system design and operation.

2.2.6 Hughes Report, "Function and Configuration Analysis Program", October 1976 - The objective of this study was to perform an investigation into the feasibility, practicability and implementation of a standard electronic module (SEM) program for avionics. The data gathered, the conclusions reached and

the recommendations made during this study are included in the report. Several possible module configurations were analyzed with four primary areas of interest being: physical characteristics, power capabilities, components and module interface. The 7 recommended module sizes, compatible with ATR packaging, are:

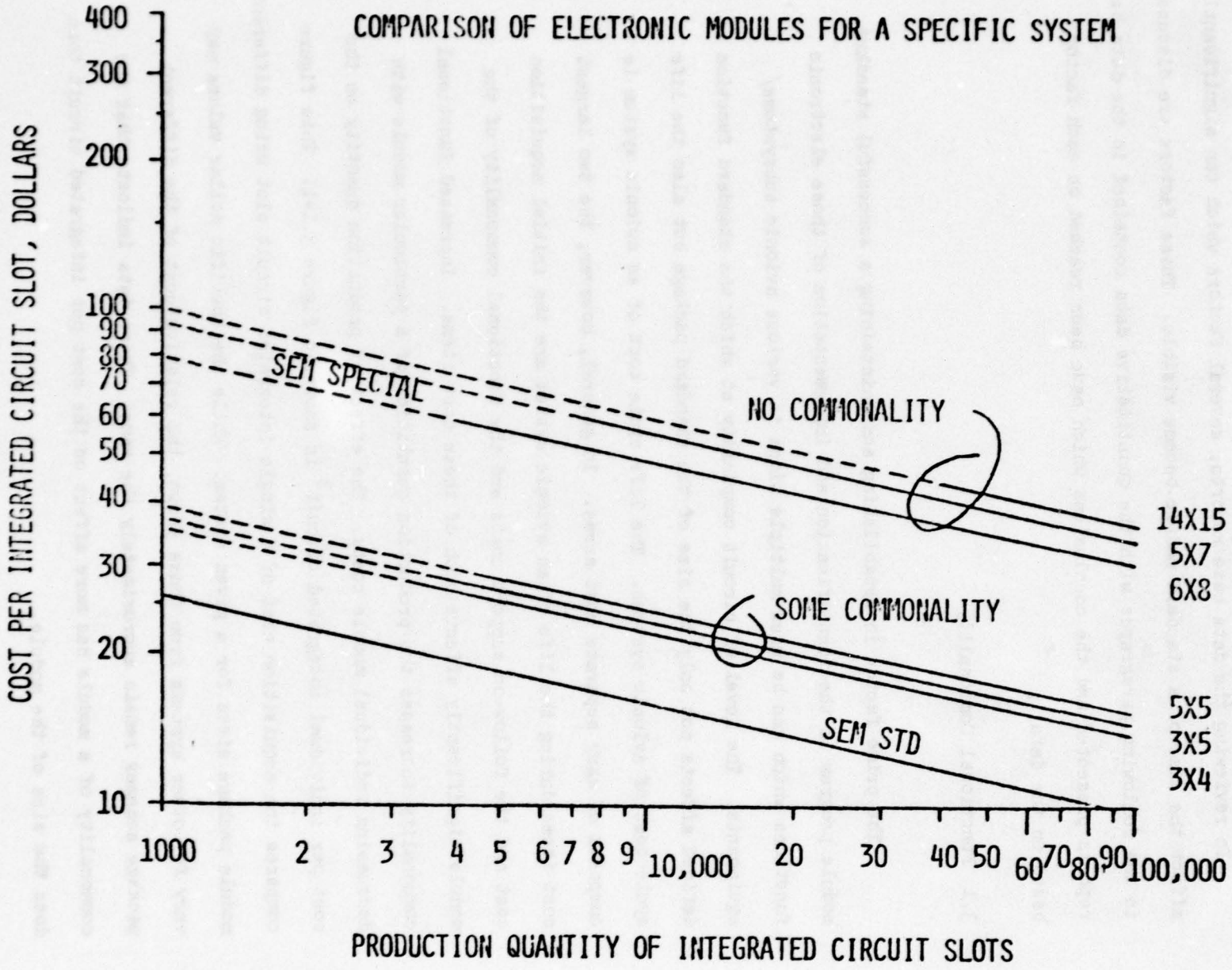
LRU PACKAGE	I/O CONTACTS	MAX POWER CAPABILITY (WATTS)	MODULE SIZE HEIGHT	MODULE SIZE WIDTH
1/2 ATR	168	35	3.40"	5.12"
	220	9	3.40"	6.50"
3/4 ATR	168	65	6.00"	5.12"
	220	16	6.00"	6.50"
1 ATR	240	101	6.17"	6.91"
	300	25	6.17"	8.70"
Advanced Technology Module	300	106	5.20"	9.00"

3.0 FACTORS AFFECTING MODULE SIZE

In reviewing the data base reports, several factors which can significantly affect the size of a standard module became visible. These factors are discussed in the following paragraphs with the quantitative data contained in the data base reports presented and the conclusions which have been reached on each factor based on the data.

3.1 Functional Commonality

The prime factor in establishing and maintaining a successful standard module program is the identification and implementation of those electronic functions which can be used multiple times in various avionic subsystems/ equipments. The level of circuit complexity at which the standard function is defined affects not only the size of the standard package but also the life cycle cost of avionic systems. The life cycle cost of an avionic system is composed of many separate cost areas. In general, however, the two largest cost items during the life of an avionic system are the initial acquisition cost and the follow-on support costs and the functional commonality of the module significantly affects both of these cost items. Increased functional commonality increases the production quantities of a particular module with decreasing individual module costs. The effect of production quantity on the cost per individual integrated circuit[3] is shown in Figure 3.1-1. This figure compares the acquisition cost of a single integrated circuit slot using different module package sizes for a given system. While the specific dollar values may vary for other systems from those shown, the relative cost of the different package schemes remain approximately the same. These data indicate that the commonality of a module has more affect on the cost per integrated circuit than does the size of the module.



REF: NAFI TR 2146

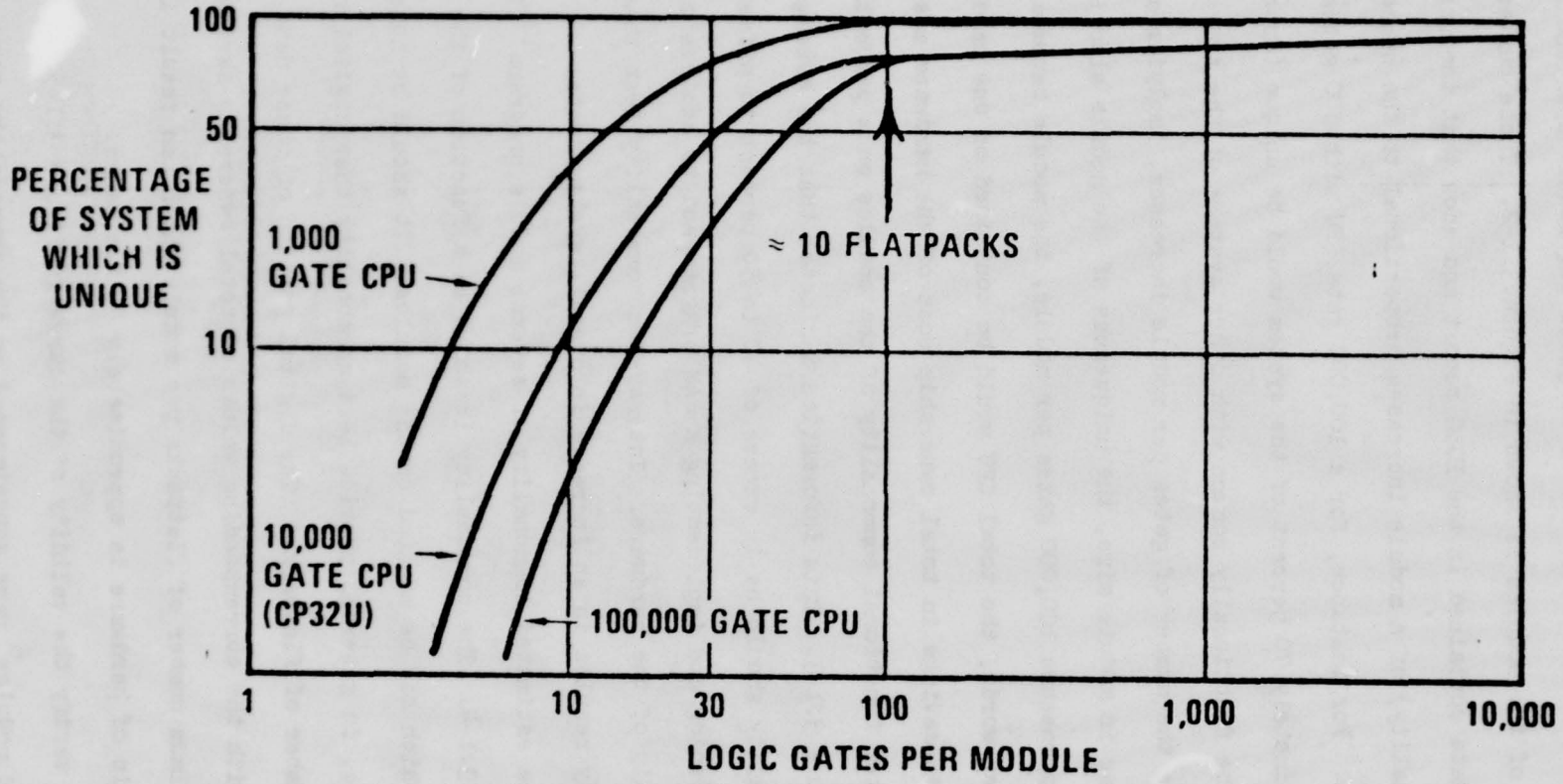
FIGUI 3.1-1

The effect of the number of gates per module upon the functional commonality of the modules is shown in Figure 3.1-2. These curves are taken from G.E. data contained in the EG&G report and show that the uniqueness (inverse of commonality) of a module increases proportional to the number of gates on the module. For instance, for a 100,000 gate CPU with 100 gates per module, approximately 70 percent of the system would be unique (approximately 30 percent would be functionally common with other systems of the same type). For this CPU, as the number of gates per module increases, implying a corresponding increase in module size, the uniqueness of the module also increases. As the size approaches 100,000 gates per module, the module becomes totally unique. In other words, the total CPU would be contained on one card or module.

The savings in total ownership cost of the hardware associated with system to system functional commonality of the modules on a percentage basis[12] is shown in Figure 3.1-3. This information indicates that the average intersystem module commonality should be in excess of 40 to 50 percent to offset the cost of establishing and implementing a SAM program and to achieve cost savings in the ownership of the hardware. Intersystem commonality less than 35 percent actually results in an increase in overall system costs.

The estimated commonality of several module programs[12] is indicated in Figure 3.1-4. The commonality is shown as a function of the number of flatpacks which can be mounted on the modules. It should be noted that analog circuits, in general, provide less commonality than digital circuits with the same number of flatpacks. The digital portion of these data is shown on Figure 3.1-5 with the corresponding values of total ownership savings and shows that the maximum number of flatpacks per module which can result in savings in total ownership of hardware is approximately 30 flatpacks.

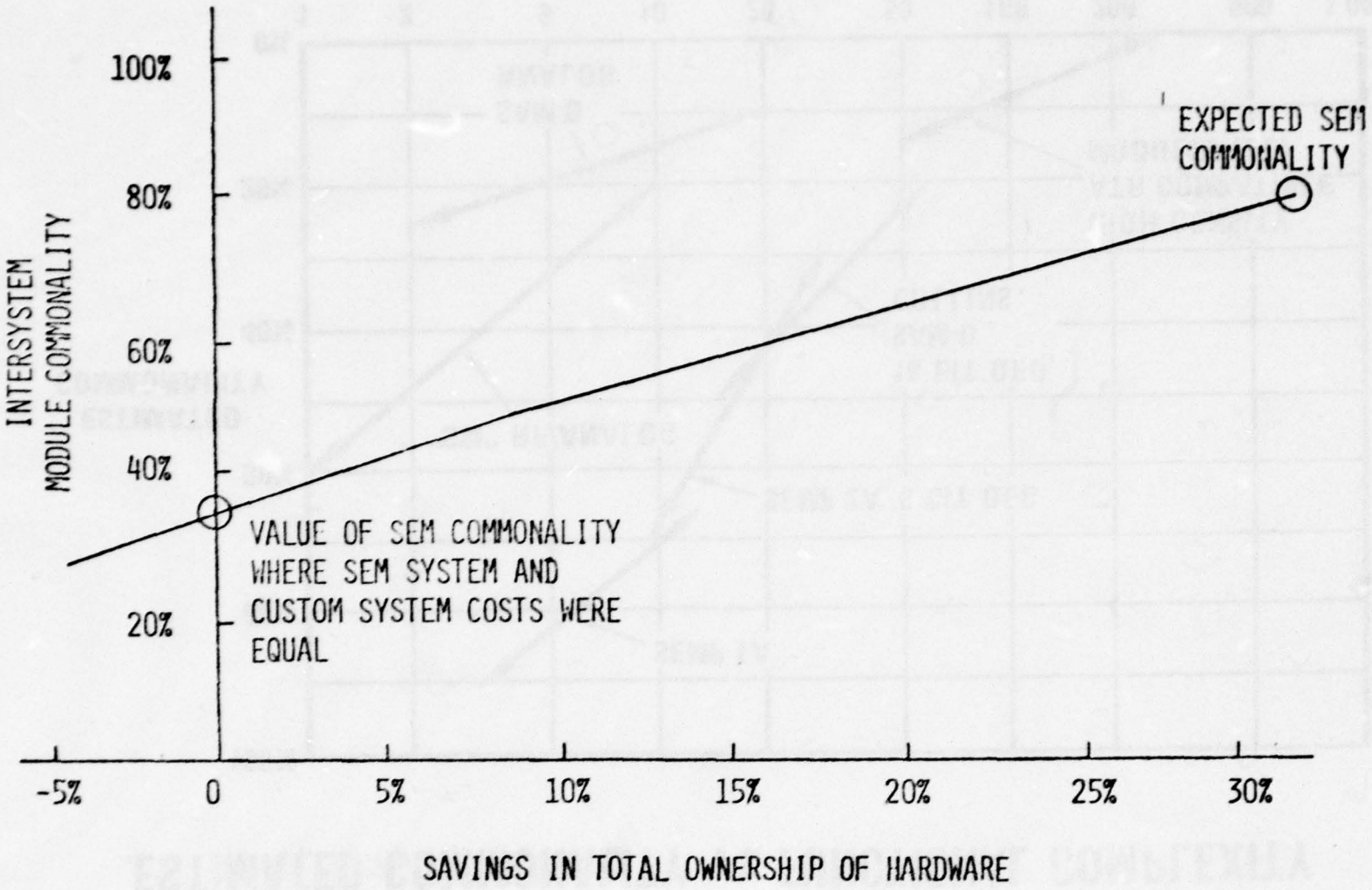
To verify the validity of the curve in Figure 3.1-5, several potential standard modules[6] were superimposed on the commonality curve. This information



REFERENCE: EG&G REPORT (GE DATA)

FIGURE 3.1-2

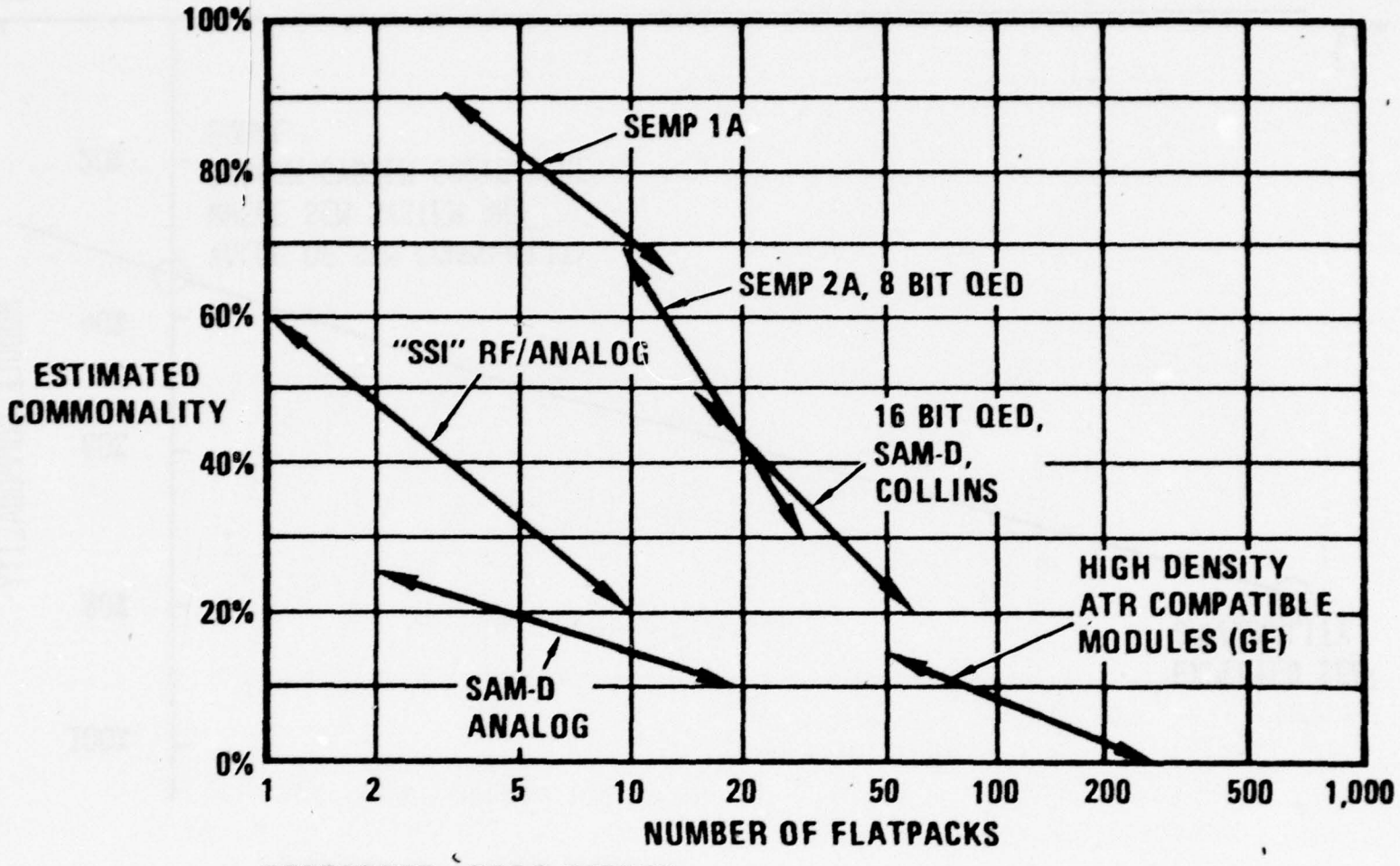
P7-1655-10



REF: EG&G REPORT

FIGURE 3.1-3

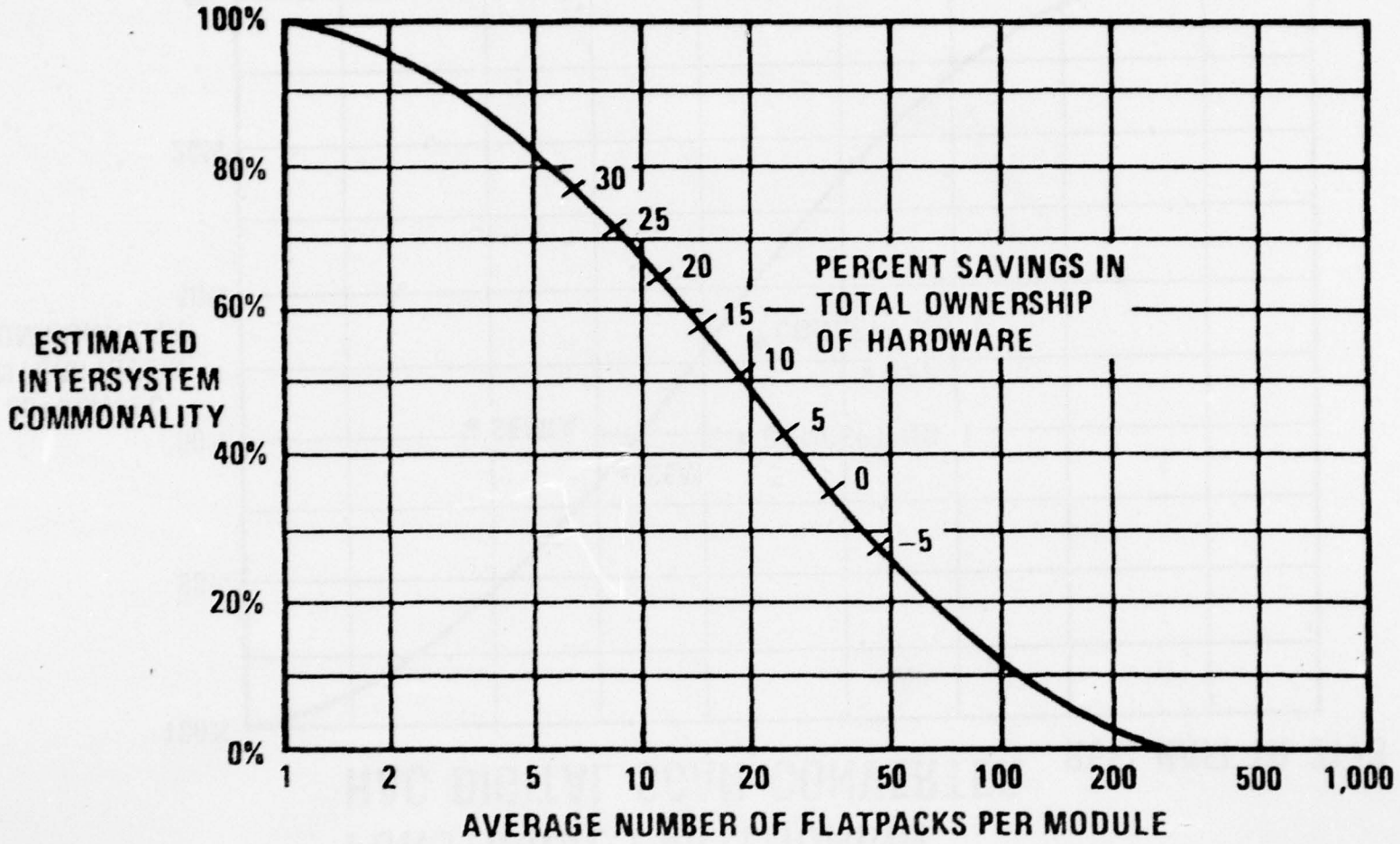
ESTIMATED COMMONALITY vs FUNCTIONAL COMPLEXITY



REFERENCE: EG&G REPORT

FIGURE 3.1-4

INTERSYSTEM COMMONALITY vs FUNCTIONAL COMPLEXITY



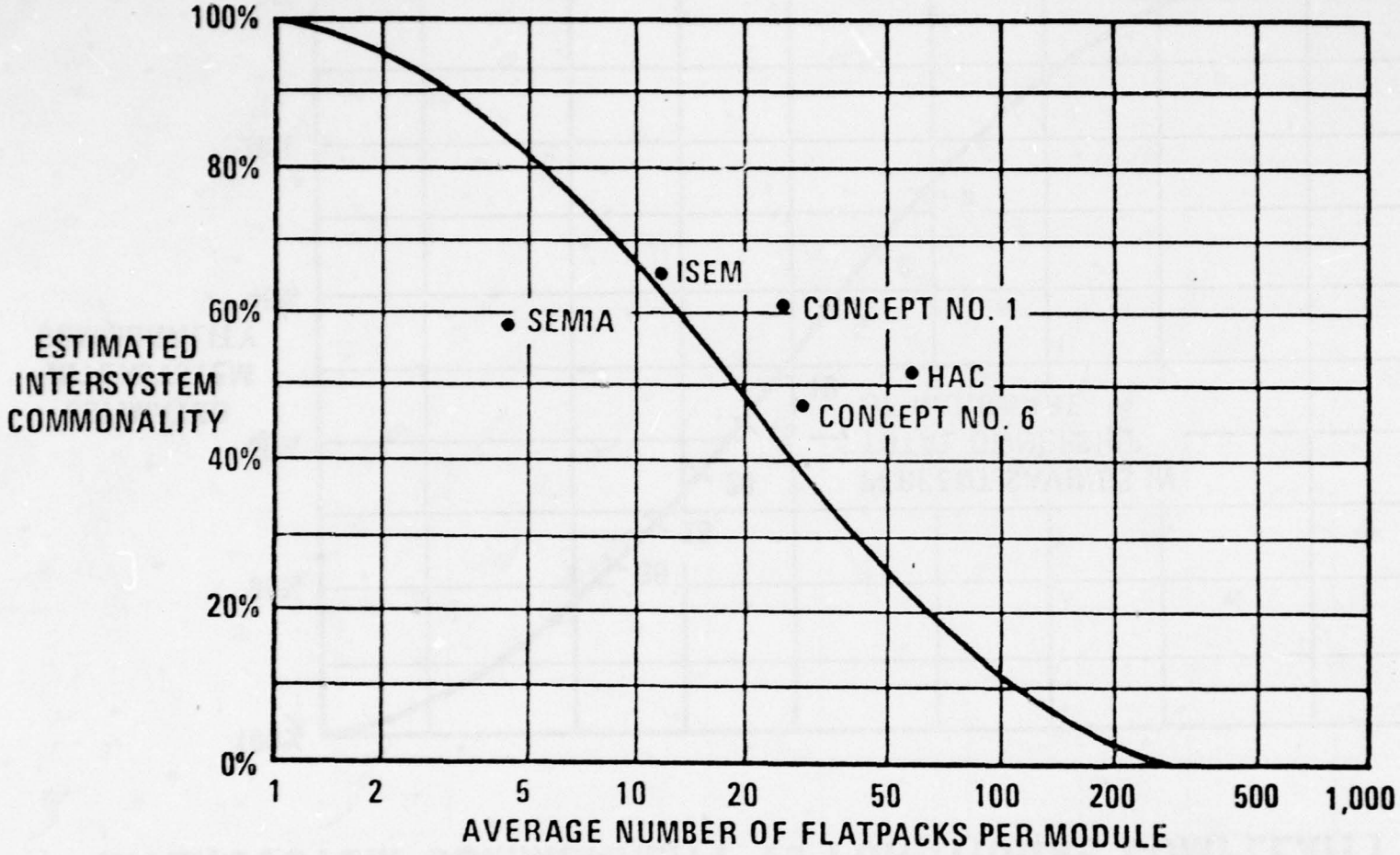
REFERENCE: EG&G REPORT

P7-1866-12

FIGURE 3.1-5

POTENTIAL STANDARDS
FUNCTIONAL PARTITIONING
HAC DIGITAL SCAN CONVERTER

REF: NAFI TR 2173



BASED ON 0.3 IN.^{2}/FP AND
55% COMPONENT PACKAGING
EFFICIENCY

P7-1655-13

FIGURE 3.1-6

is shown in Figure 3.1-6. These data, taken from the NAFI TR 2173 report, were derived from a study which partitioned the Hughes Digital Scan Converter into distinct functions which could be packaged within selected module physical constraints. The packaging analysis was based upon 0.3 square inches per flatpack and a 55% packaging efficiency. The intersystem commonality was estimated for each board or module based upon the function of the board and experience with other system requirements.

The conclusions reached in the analysis of the effects of functional commonality is that, based upon the considerations of the data base and reference studies, the maximum number of integrated circuits which should be provided on a standard module to realize any cost savings in life cycle costs is 30.

3.2 Connector Selection

Since both the width and the thickness of the module is essentially determined by the dimensions of the connector which interfaces electrically between the module and the back plane wiring or mother board, the selection of the connector including the number of pins and the pin type is of paramount importance in determining the size of a standard module.

3.2.1 Number of Pins

Two possible methods of calculating the number of pins required to interface a functional circuit with the rest of the subsystem are provided by G.E. in the EG&G report.[12] These two methods are (1) based upon the number of integrated circuits (IC) included in the circuit;

$$\text{NO. PINS} = C\sqrt{IC} \qquad \text{(EQ. 3.2-1)}$$

where C is between 12 and 18

and (2) based upon the number of logic gates included in the circuit;

$$\text{NO. PINS} = 3.8\,G^{r} \qquad \text{(EQ. 3.2-2)}$$

where G is the number of gates and r is dependent upon the functional complexity of the circuit as follows:

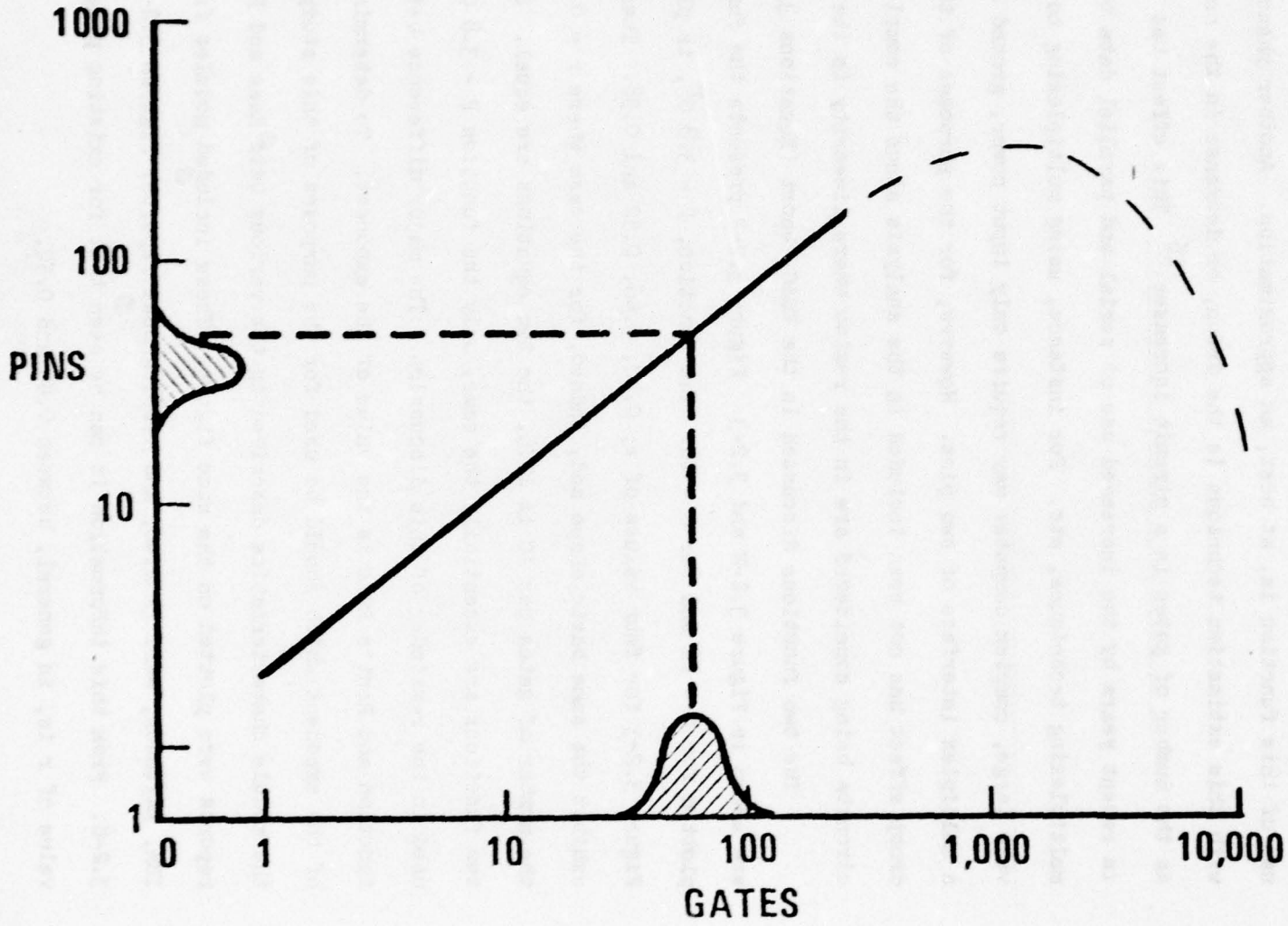
r	complexity
.58	High
.52	Nominal
.46	Low
.40	Extremely low

These two equations are based upon an empirical function known as Rent's Rule shown in Figure 3.2-1. This is a function evolved[15] to estimate the number of connections required for electronic systems. This function is valid whether the circuit under consideration is a total functional equipment, a circuit board or an individual IC. It should be noted that the number of

RENT'S RULE

(EMPIRICAL)

NO. PINS = aG^r WHERE a IS ABOUT 4, r IS ABOUT 2/3



P7-1655-1

FIGURE 3.2-1

pins determined by this function is not necessarily a specific value since there is a probability distribution associated with the result. For these reasons, the use of this function is, at best, an approximation. Another phenomenon associated with this estimation technique is the droop, or decrease in the number of pins, as the number of gates in a circuit increases.[16] This effect has been experienced in recent years by the increased use of serial and parallel data bus architectures, multiplexing techniques, etc. For instance, using multiplexing to its fullest, a very large, complex computer may require only input power, ground and possibly a multiplex interface of two pins. However, for the purposes of this study, this droop effect has not been included in the analysis since the complexity of the circuits being considered are in the region where linearity in the curve exists.

The two functions discussed in the EG&G report (Equations 3.2-1 and 3.2-2) are shown in Figure 3.2-2 and 3.2-3. Figure 3.2-2 presents the function $P = C\sqrt{IC}$, plotted for C = 12 and for C = 18. The function, $P = 3.8\ G^r$, is plotted in Figure 3.2-3 for four values of r; 0.40, 0.46, 0.52 and 0.58. These two functions exhibit the same basic shape and, indeed, for the case where r = 0.5, C = 16 and the number of gates per IC is 17.8, the two equations are equal. Since these two functions are essentially the same, only the function $P = 3.8\ G^r$ will be used in the remainder of this discussion. The major difference between this function and Rent's Rule is the value of the exponent. To determine the value of the exponent which should be used for the purposes of this study; several of the module characteristics described in the various Data Base and Reference reports were plotted on the same figure. These included modules from the Hughes, IBM, Raytheon, NAFI TR 2146, and Westinghouse reports, Figures 3.2-4 through 3.2-8. From this information it can be seen that for existing programs, the value of r is, in general, between 0.46 and 0.52.

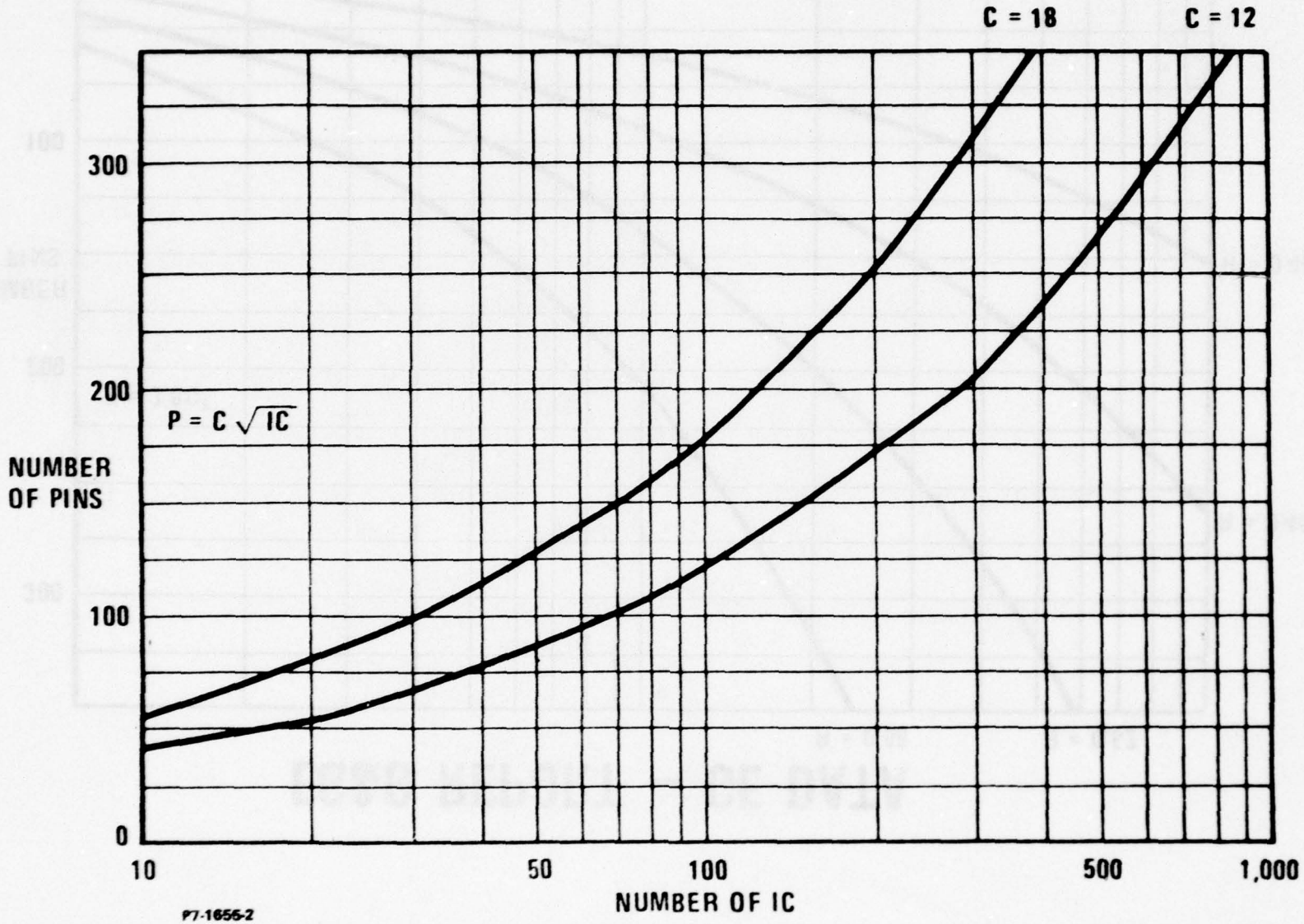
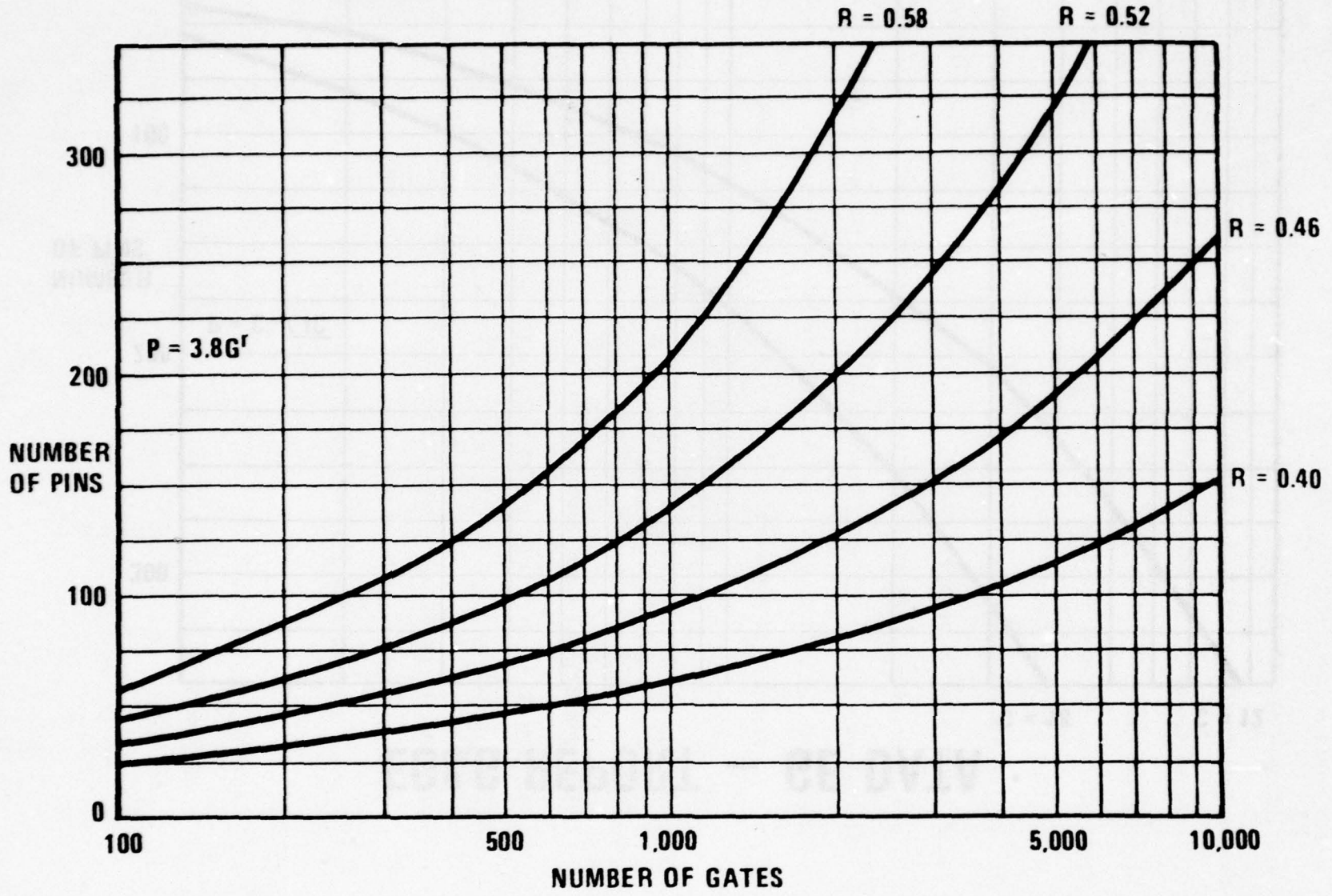

EG&G REPORT – GE DATA
C = 18
C = 12
300
200
100
0
P = C √IC
NUMBER OF PINS
10
50
100
500
1,000
NUMBER OF IC
P7-1656-2

FIGURE 3.2-2


EG&G REPORT – GE DATA
R = 0.58
R = 0.52
R = 0.46
R = 0.40
P = 3.8G^r
300
200
100
0
NUMBER OF PINS
100
500
1,000
5,000
10,000
NUMBER OF GATES
P7-1855-3

FIGUR 3.2-3

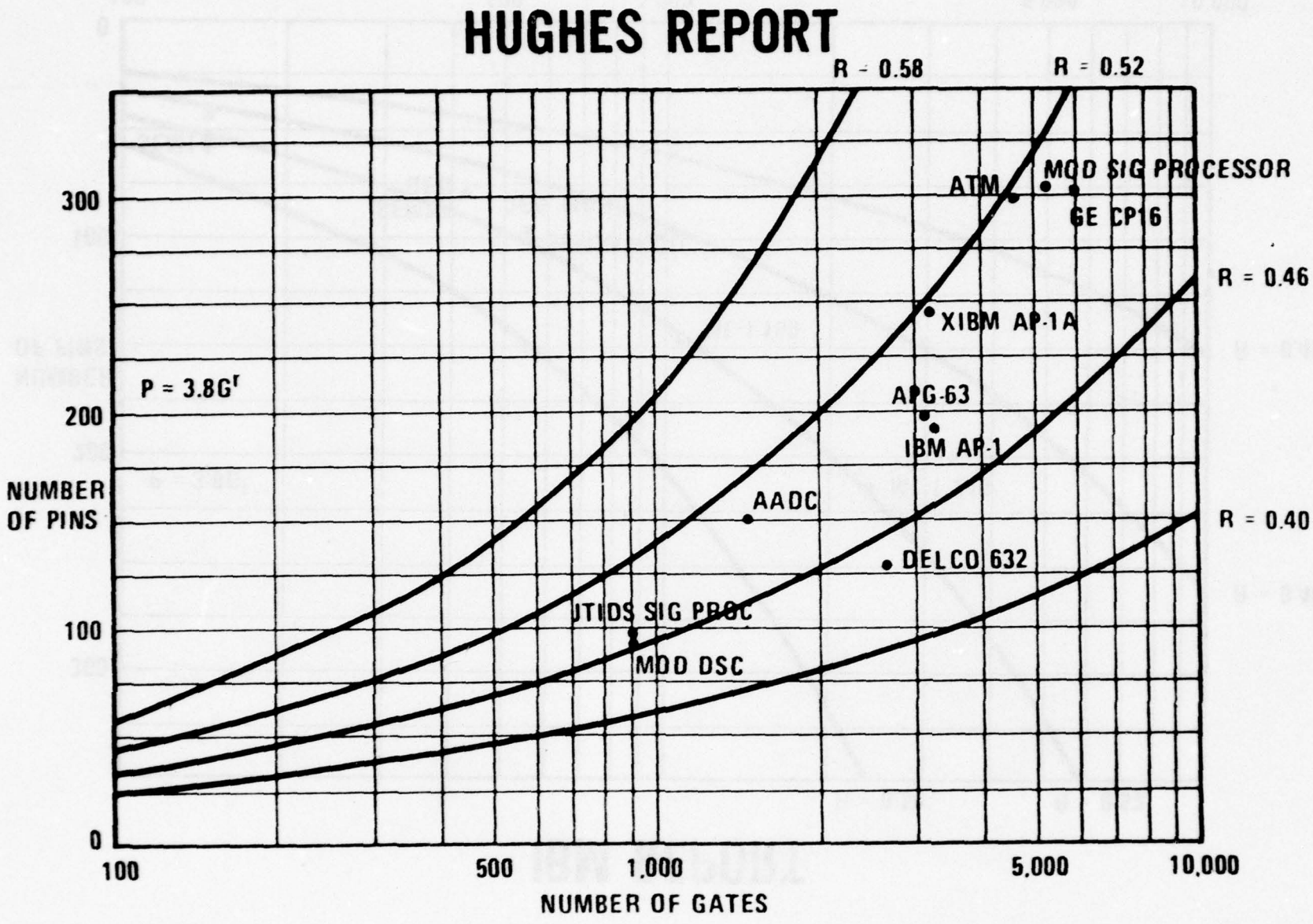

HUGHES REPORT
R = 0.58
R = 0.52
R = 0.46
R = 0.40
P = 3.8G^r
ATM
MOD SIG PROCESSOR
GE CP16
XIBM AP-1A
AYK-63
IBM AP-1
AADC
DELCO 632
JTIDS SIG PROC
MOD DSC
NUMBER OF PINS
0
100
200
300
100
500
1,000
5,000
10,000
NUMBER OF GATES
P7-1655-4

FIGURE 3.2-4

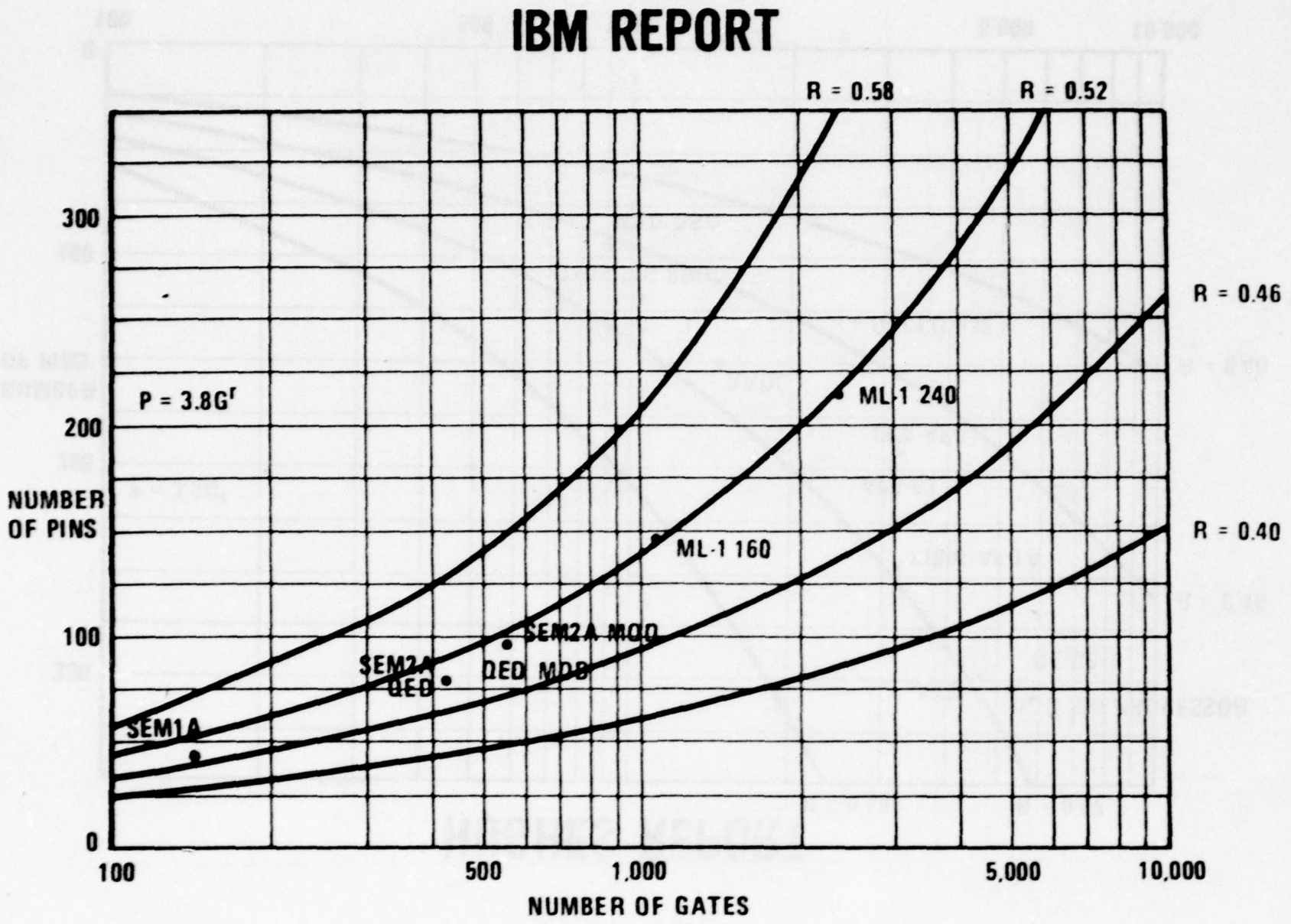
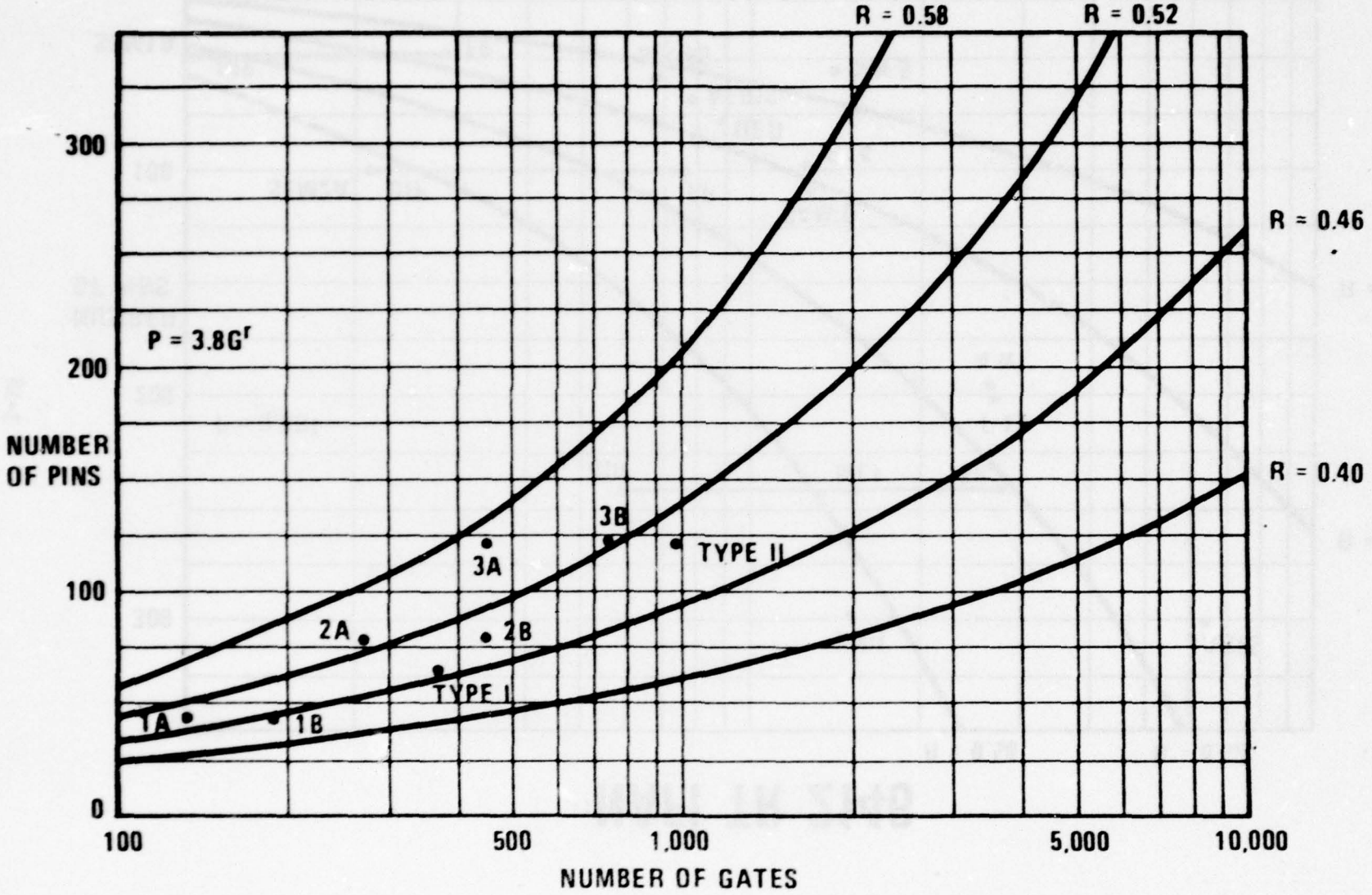

IBM REPORT
R = 0.58
R = 0.52
R = 0.46
R = 0.40
P = 3.8G^r
ML-1 240
ML-1 160
SEM2A MOD
SEM2A QED MOD
SEM2A QED
SEM1A
300
200
100
0
NUMBER OF PINS
100
500
1,000
5,000
10,000
NUMBER OF GATES
P7-1055-6

FIGURE 3.2-5

RAYTHEON REPORT



P7-1655-6

FIGURE 3.2-6

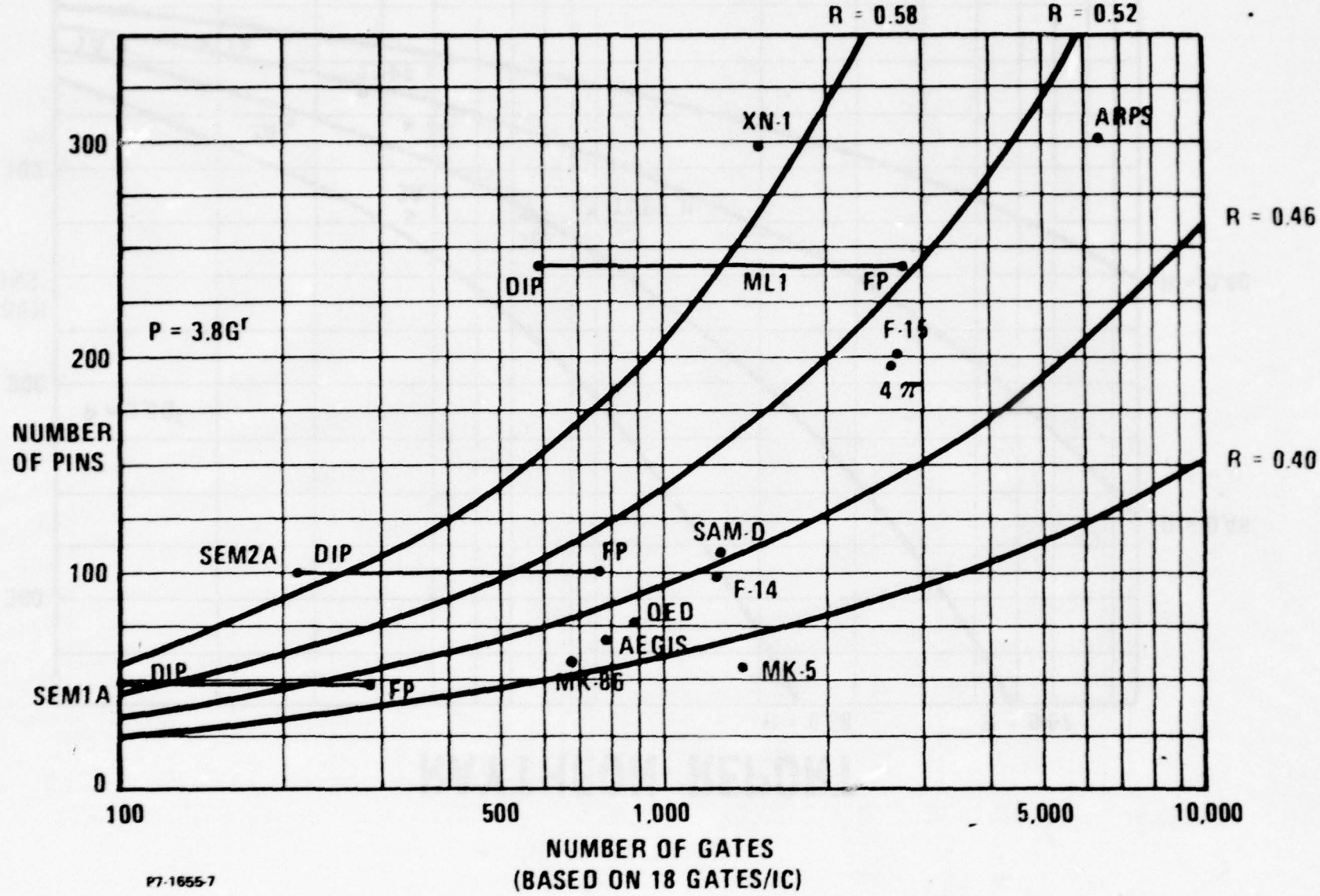

R = 0.58
R = 0.52
R = 0.46
R = 0.40
XN-1
ARPS
DIP
ML1
FP
P = 3.8G^r
F-15
4 π
SEM2A
DIP
FP
SAM-D
F-14
QED
AEGIS
MK-86
MK-5
SEM1A
DIP
FP
300
200
100
0
NUMBER OF PINS
100
500
1,000
5,000
10,000
NUMBER OF GATES
(BASED ON 18 GATES/IC)
P7-1655-7

FIGURE 3.2-7

WESTINGHOUSE REPORT

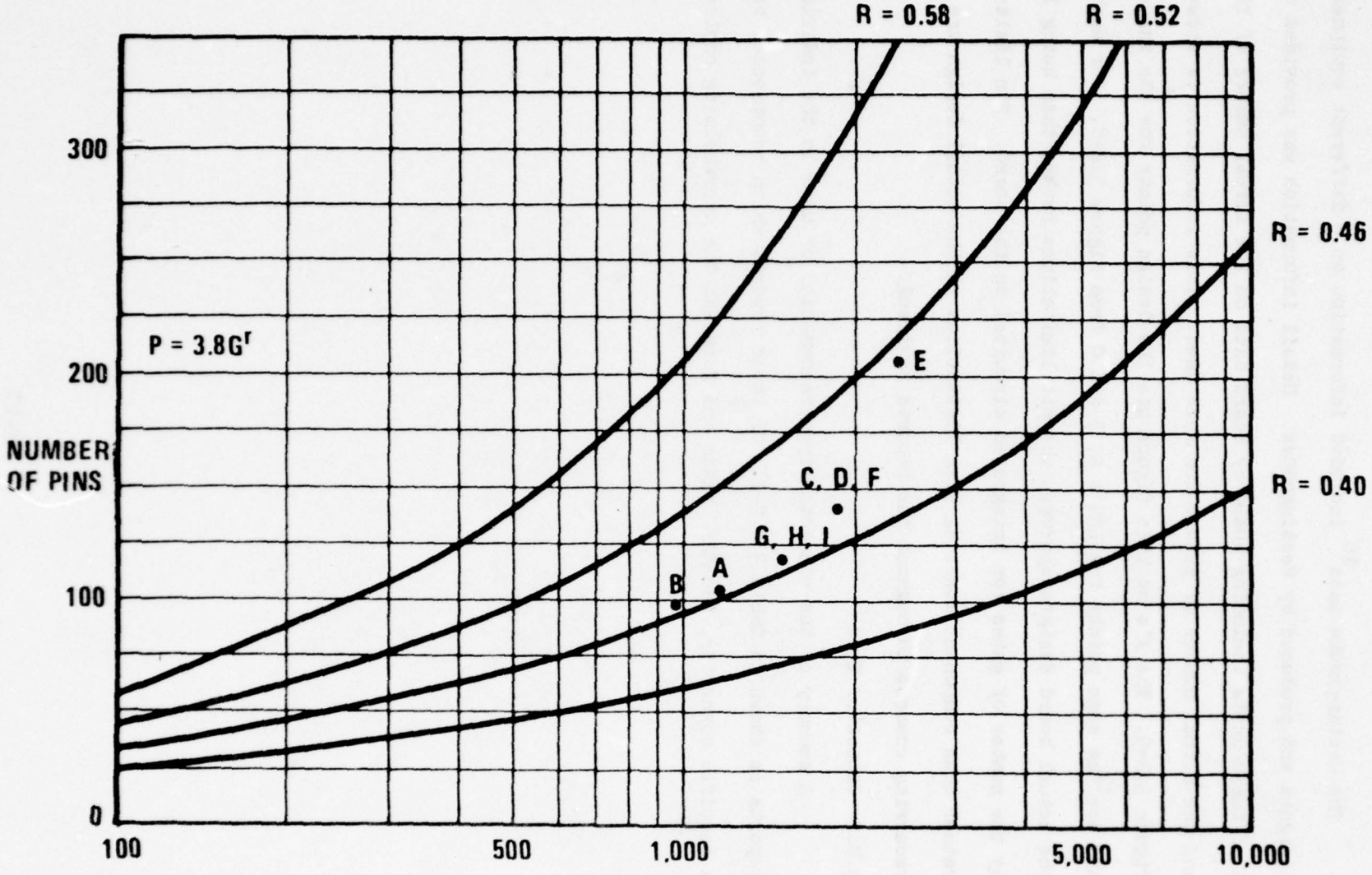


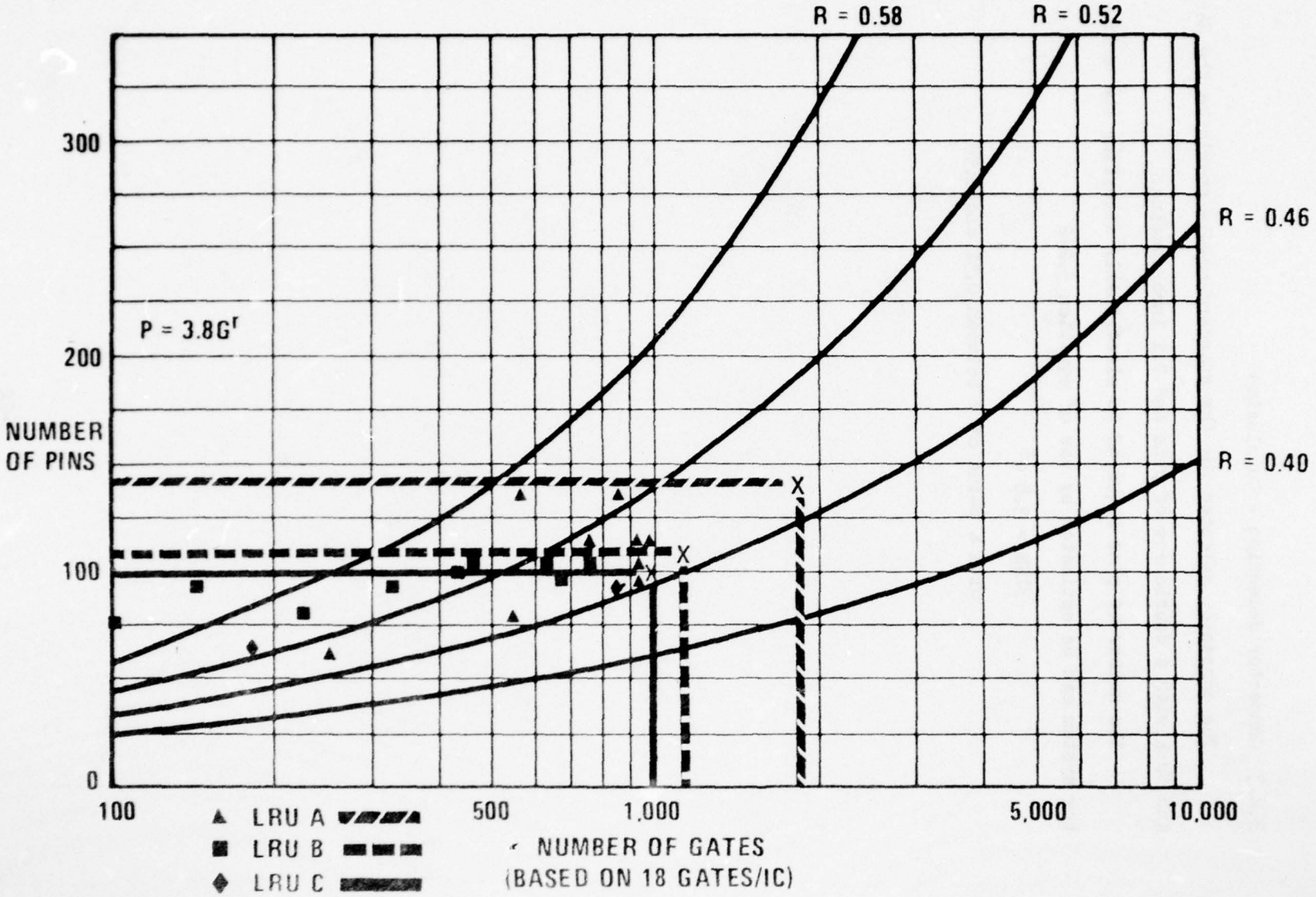
FIGURE 3.2-8

The Westinghouse data[10] included information on 9 different equipments designed and produced by Westinghouse. Detail information was provided on 3 of these units including board by board data on the actual number of IC's and the actual number of pins which were used. This information is shown in Figure 3.2-9. The X's on this figure are the design points for the three units and are the same points for LRU's A, B and C from Figure 3.2-8. For each LRU, the actual board designs approach the pin limitations rather than being limited by the number of gates (or integrated circuits) on the board. Pin limitations rather than component mounting area limitations in the actual design are a recurring comment throughout the reports reviewed.

3.2.2 Connector Type

A summary of the connector type recommended or used in the individual reports is shown in Table 3.2.2-1. Of those reports which recommended or used a specific connector, the NAFI blade and fork was the overwhelming choice.

WESTINGHOUSE REPORT



P7-1655-9

FIGURE 3.2-9

3.2.3 Connector Selection - Conclusion

The connector selected for the standard module should be the NAFI blade and fork with a double row of pins and 0.1 inch spacing.

The number of pins required to electrically interface the module into the system can be estimated by use of equation 3.2-2

$$PINS = 3.8\ G^{r}$$

with a value of r between 0.52 and 0.58

TABLE 3.2.2-1

CONNECTOR TYPE

REPORT	CONNECTOR
HONEYWELL	--
GE	--
RAYTHEON	NAFI
TELEPHONICS	--
NAFI	--
NADC	NAFI
WESTINGHOUSE	NAFI
HUGHES	NAFI
EG&G	NAFI
IBM	NAFI
DMSSB	--

3.3 Integrated Circuit Technology

3.3.1 Component Packaging

Several of the reports contained projections of the integrated circuit which might be expected for a standard module program.

The Westinghouse report[10] did not project into the 1985 time frame but provided packaging capabilities in the recommended modular packaging concept for DIP, flatpack, bare chips and discrete components.

The Hughes packaging study[14] selected the flatpack configuration over the DIP because:

a. Less weight and volume

b. Fewer modules required

c. Lower mean case operating temperatures

d. Resultant lower life cycle costs

The IBM study[9] included trade-offs between the DIP and the flatpack devices in the areas of volume, manufacturing cost/process, future availability and optimum module sizes. As part of the study a survey was made to project availability of the integrated circuit packages in the early 1980 time frame. The companies contacted were:

Advanced Micro Devices (AMD)

Motorola

Monolithic Memories, Inc.

Texas Instruments

- Digital Military Marketing
- Linear Marketing

The conclusions reached in the IBM report were:

- Flatpacks offer volumetric advantage
- DIP's require less processing to mount and attach

- DIP's offer cost advantage at component level
- DIP packages will be more widely used than flatpacks
- Devices requiring 24 pins or less will be available in both flatpack or DIP
- Devices requiring more than 24 pins will be available almost exclusively in DIP
- 40 pin DIP appears to be industry standard for complex devices
- Possible introduction of DIP packages in 20 to 80 pin configuration
- Larger DIP packages may use staggered lead pattern

The NAFI TR 2146 study[3] examined projected commercial microelectronic device packaging in the 1980 time frame. The projected future usage of the packages examined, indicated the priority of packages as shown in Table 3.3.1-1 with DIP packages more widely used than flatpacks. The report also concludes that the advent of larger large scale integration (LSI) chips will hasten the increased use of other packages such as the leadless carrier.

The leadless chip carrier and other similar packaging techniques are not discussed in any significant detail in the Data Base and Reference Reports since most were completed prior to the emergence of these technologies. At the present time, the chip carrier is being actively discussed in the literature with most of the articles prepared by manufacturers of the devices. The chip carrier is much smaller and weighs less than the DIP, as shown in Table 3.3.1-2, but there are several areas of concern in defining, at the present time, a standard module program for the mid 80's based upon complete use of a technology such as the chip carrier. These concerns are:

a. Reliability, inspectability and repair of the solder joints.

b. Power dissipation of a module using high density packaging.

TABLE 3.3.1-1

INTEGRATED CIRCUIT PACKAGES
NAFI TR 2146
SEPT. 1976

PRIORITIZED LIST OF PACKAGES

DIPS	14 - 16 PIN
	24
	28
	40
FLAT PACKS	14 - 16 PIN
	24
	40
METAL CANS	TO - 5
	TO - 3
	TO - 8
HYBRIDS	
LEAD LESS HYBRIDS	

TABLE 3.3.1-2

CHIP CARRIER/DUAL IN-LINE
PACKAGE COMPARISON

I/O COUNT	AREA (SQUARE INCHES)			WEIGHT (GRAMS)		
	CHIP CARRIER	DIP	RATIO	CHIP CARRIER	DIP	RATIO
16	0.0324	0.24	7.4	0.0502	1.1474	22.9
18	0.0625	0.27	4.3	0.1337	1.3666	10.2
24	0.1122	0.72	6.4	----	----	----
28	0.1600	0.84	5.3	0.3315	4.0159	12.1
40	0.2116	1.20	5.7	----	----	----
48	0.2500	2.16	8.6	0.4994	9.0000	18.0
64	0.5184	2.80	5.4	1.6288	12.1120	7.4

REFERENCE: "CHIP CARRIERS AS A MEANS FOR HIGH-DENSITY PACKAGING",
J. S. PROKOP AND D. W. WILLIAMS, TEXAS INSTRUMENTS.

c. Thermal coefficient of expansion differences between chip carrier and module board if ceramic board is not used. The use of a ceramic board complicates the assembly of circuits which require discrete components such as capacitors, resistors, inductors and power transistors. The distribution of components used in the Integrated Electronic Warfare System (IEWS)[5], shown in Table 3.3.1-3, indicates that 10% of the components may be discretes.

d. Availability of devices in sufficient quantities and at competitive prices in the market place to enable commitment of a design to the chip carrier. This requires resolution of the following factors in a time frame compatible with the SAM schedule.

- Revision of MIL-M-38510 and other military specifications to include the chip carrier form factor and to incorporate other changes as required
- Component manufacturers who are willing to provide IC's in chip carrier package and, for military programs, to obtain listing on Qualified Parts List (QPL)
- A majority of commercial and military equipment manufacturers, involved in programs not necessarily associated with the standard module program, who are willing to fund new tooling, test and assembly equipment and who will procure chip carrier IC's in sufficient quantities and varieties to induce competitive pricing with DIP's.

The satisfactory resolution of these concerns is a difficult and perhaps lengthy process. Several of the technologies which looked promising in the recent past such as flip chip and beam lead were not able to overcome these and other difficulties and none have become widely accepted or used. Although the chip carrier looks favorable and may overcome the anticipated difficulties by the 1985 time frame, there is a significant risk associated with a commitment to establish a standard module program based totally upon the chip carrier technology.

TABLE 3.3.1-3

COMPONENT DISTRIBUTION
RAYTHEON REPORT
FEBRUARY 1977

CIRCUITS OTHER THAN RF

COMPONENT TYPE	PERCENT
DIPS	80
FLATPACKS	5
HYBRIDS	5
DISCRETES	10

Since the chip carrier was not addressed in the Data Base or Reference Material for this study, and to provide a conservative, low risk study result, the chip carrier and its use will not be addressed in significant detail in the remainder of this report.

The conclusion reached during this portion of the study is that the packaging concept which is finally selected for the SAM program must be compatible with all popular types of component packages including:

DIPS

Flatpacks

Hybrids

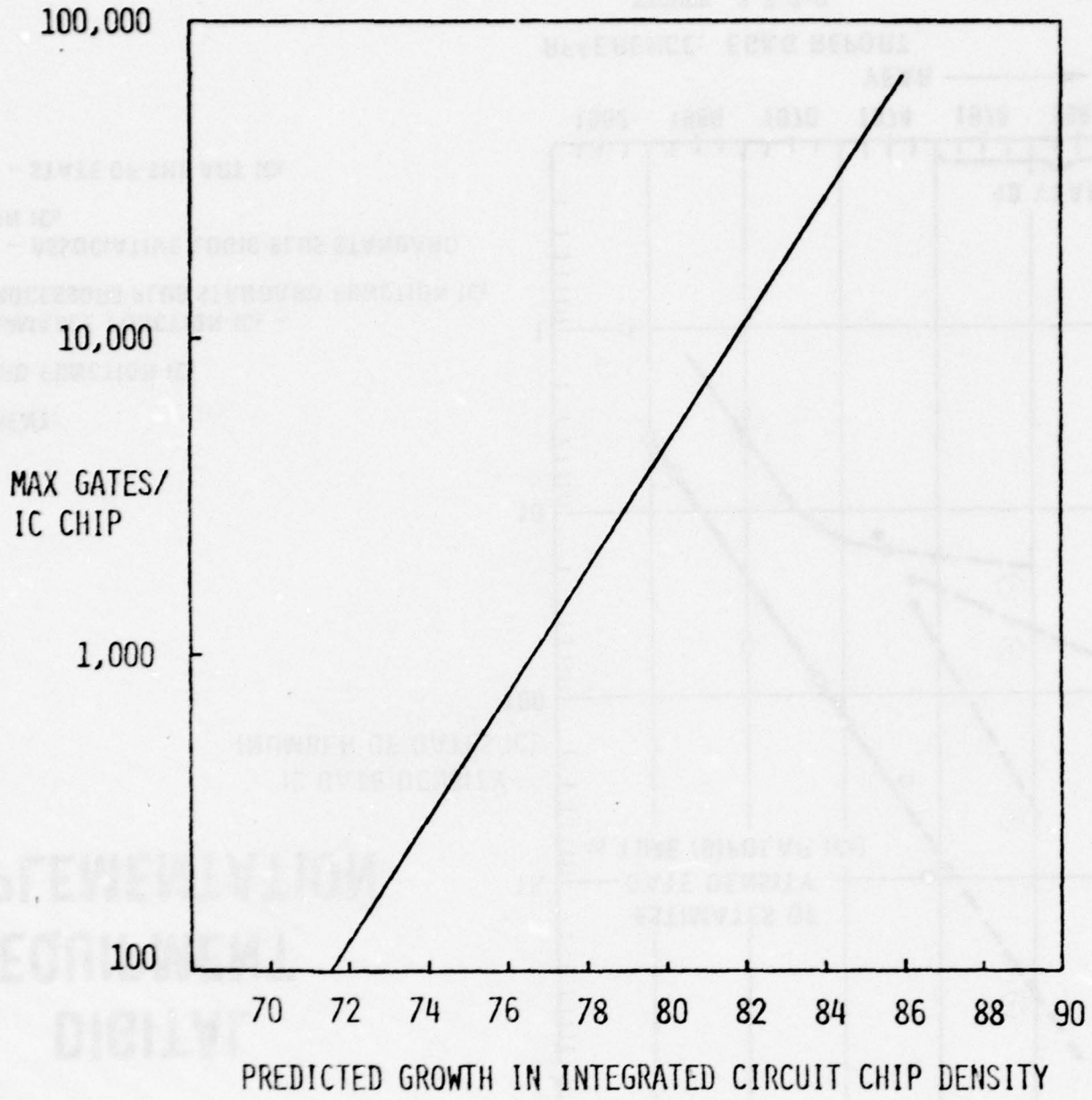
Discretes

Leadless Chip Carriers

This capability must be provided to enable the module designer to produce an acceptable circuit within the considerations of cost, weight, volume, reliability and availability of components.

3.3.2 Integrated Circuit Packaging Density

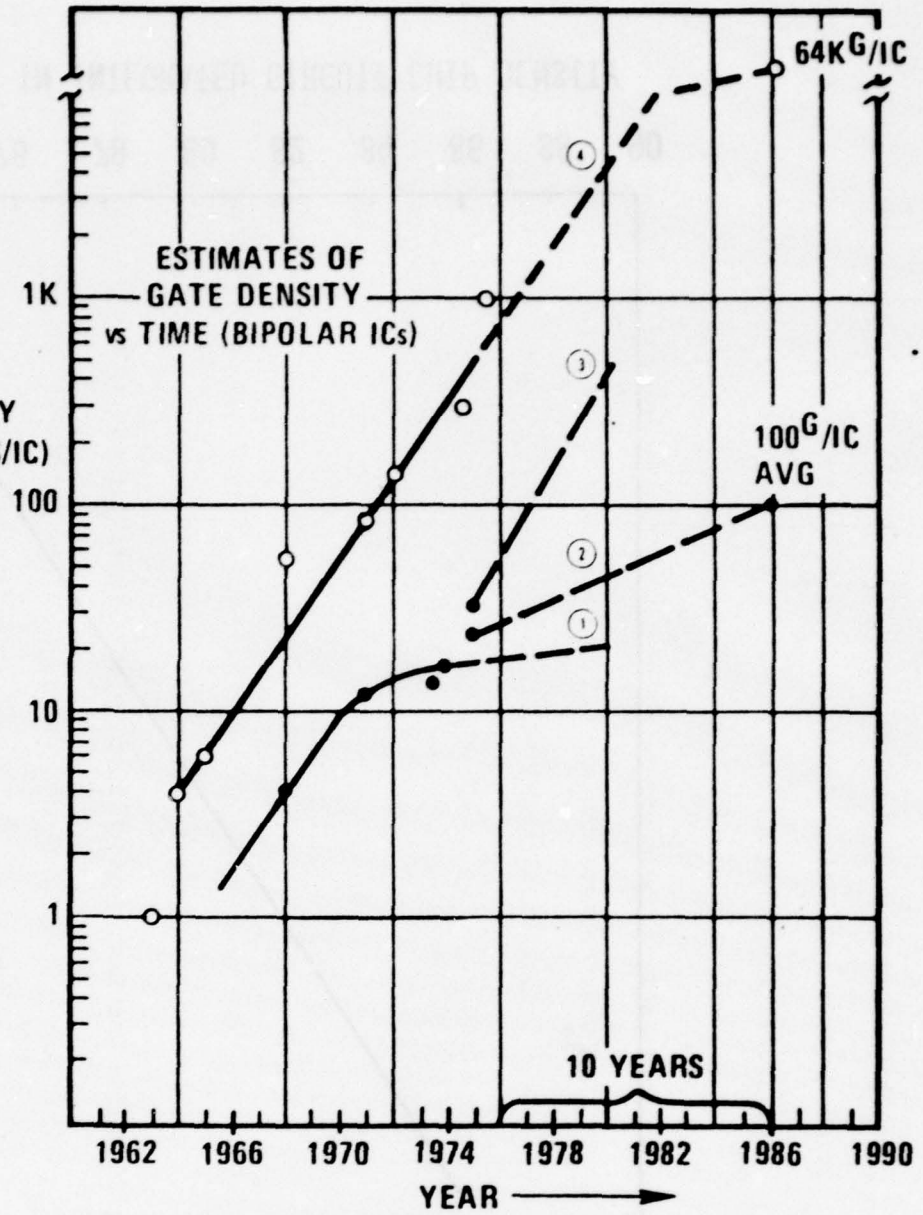
Quantitative data on the packaging density, i.e., gates per integrated circuit, which exists in present day components and the packaging density projected to exist in future components is included in the Westinghouse, EG&G and the IBM reports. The Westinghouse report[10] provides data on the predicted growth in integrated circuit chip density as shown in Figure 3.3.2-1. These data indicate that the maximum number of gates per chip in 1977 were on the order of 1500 to 2000 gates and will increase by 1985 to a maximum of approximately 70 K gates. It should be noted that these are a maximum or upper limit and is not indicative of the average number of gates per chip. A similar datum is shown in Curve 4 of Figure 3.3.2-2 taken from the EG&G report.[12] This figure also indicates that in 1985 the average number of gates per chip will be approximately 100.



REF: WESTINGHOUSE REPORT

Figure 3.3.2-1

DIGITAL EQUIPMENT IMPLEMENTATION



ICs IN EQUIPMENT:

① STANDARD FUNCTION ICs

② PROGRAMMABLE FUNCTION ICs – MICROPROCESSORS PLUS STANDARD FUNCTION ICs

③ CUSTOM – ASSOCIATIVE LOGIC PLUS STANDARD FUNCTION ICs

④ CUSTOM – STATE-OF-THE-ART ICs

FIGURE 3.3.2-2

The distribution of the packaging density for electronic equipment (1974)[12] is shown in Figure 3.3.2-3 and indicates that the average number of gates per IC is 17.8. This estimate is supported by data from other reports. The Proteus Central Processor and Input/Output[9] is a 40,000 gate device with an average of 17.2 gates per device and dissipating 9.26 milliwatts of power per gate. Additional data are shown in Tables 3.3.2-1 and Tables 3.3.2-2 from the EG&G report and the Westinghouse report indicating an average number of gates per IC of between 9 and 20. From these it must be concluded that an average of about 18 gates per IC is correct and that, further, the EG&G report data is essentially correct. An estimate of the packaging density for equipment in 1986 is shown in Figure 3.3.2-4 as taken from these same report data. This estimate indicates that the average number of gates per IC in 1986 will be 104.

It is interesting to note that using the equation to estimate pin count, Eq. 3.2-2,

$$\text{PINS} = 3.8\ G^{0.5},$$

results in the following:

17.8 GATES/IC = 16 PIN IC

104 GATES/IC = 40 PIN IC

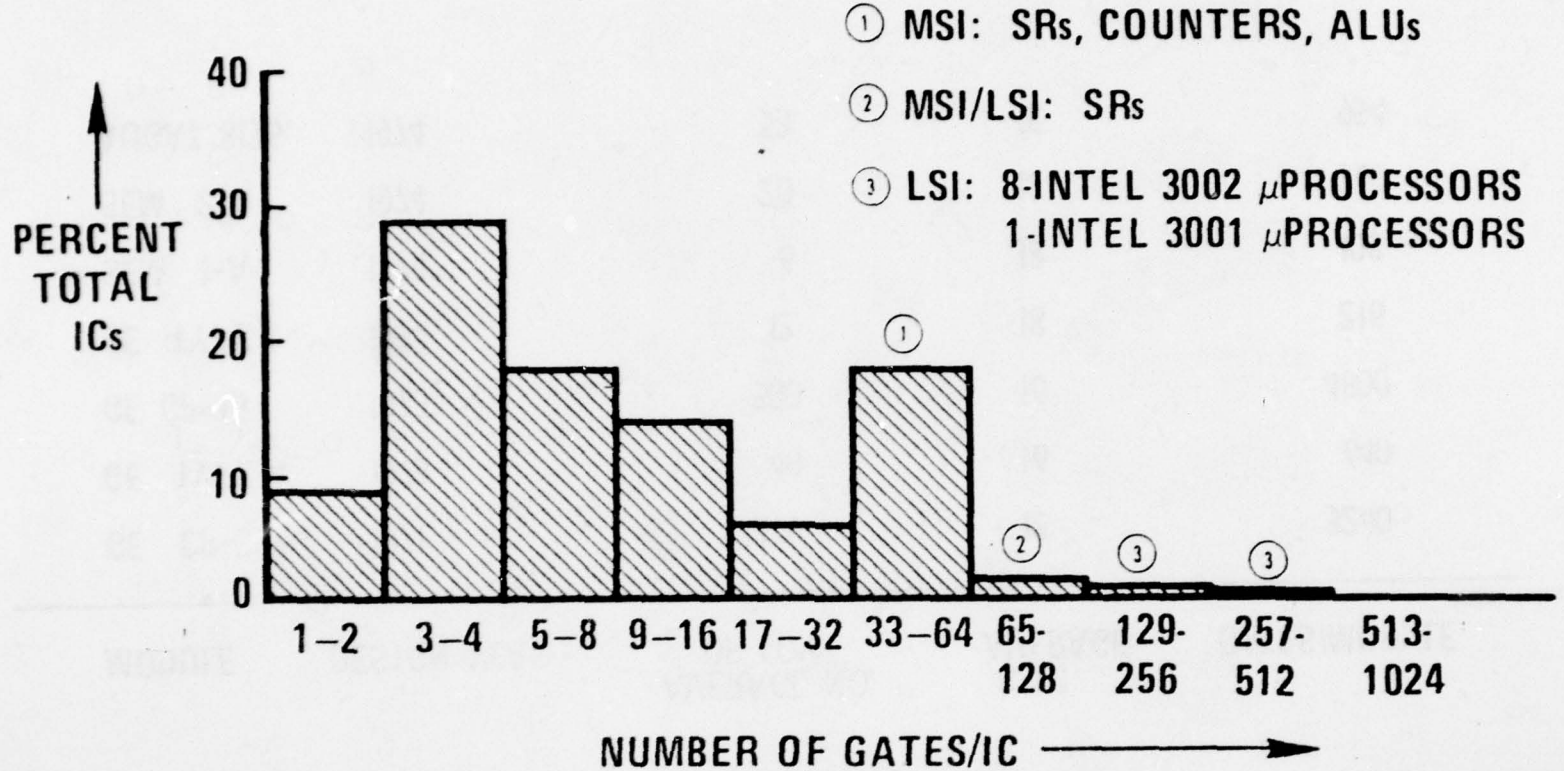
In other words, the typical IC in present technology is a 16 pin IC containing approximately 17.8 gates and the anticipated typical IC in 1985 will be a 40 pin IC containing approximately 104 gates. These characteristics will be used in the remainder of this report as reference for the typical IC.

To provide additional assurance that these average values are approximately correct, a recent design (1977) of a Stores Management Unit (SMU) being proposed for use in the A-7E was examined. The SMU is a programmable unit containing a microprocessor, core memory and associated circuitry and which performs the logical processing required to apply power to the weapons stations, to control the release of the weapons when commanded, and to provide weapons systems status to the cockpit instrument panel. The components specified for the assembly of this unit, aside from those included in the procured memory subassemblies, include 181 integrated circuits as well as several hybrid thick film modules. The integrated circuits are distributed by pin count as follows:

97	14 pin
70	16 pin
10	24 pin
3	28 pin
1	40 pin

This distribution results in a mean or average of 15.7 pins per integrated circuit which is extremely close to the above estimate of 16 pins per integrated circuit.

AVERAGE DISTRIBUTION OF ICs IN EQUIPMENT
STANDARD TTL- 1974



AVERAGE NUMBER OF GATES PER IC = 17.8

REFERENCE: EG&G REPORT

P7-1655-15

FIGURE 3.3.2-3

TABLE 3.3.2-1

IC PACKAGING DENSITY
EG&G REPORT
SEPTEMBER 1976

MODULE	DESIGN YEAR	AVERAGE NO. OF IC's	G/IC AVERAGE	GATES/MODULE
GE CP-32	1971	270	12	3240
GE TYPE 4	1973	40	16	640
GE CP-16	1973	300	16	4800
GE TYPE 1	1974	12	18	216
SEM 1-A	1974	6	18	108
SEM 2-A	1974	20	18	360
AUGAT 8136	1974	53	18	954

TABLE 3.3.2-2

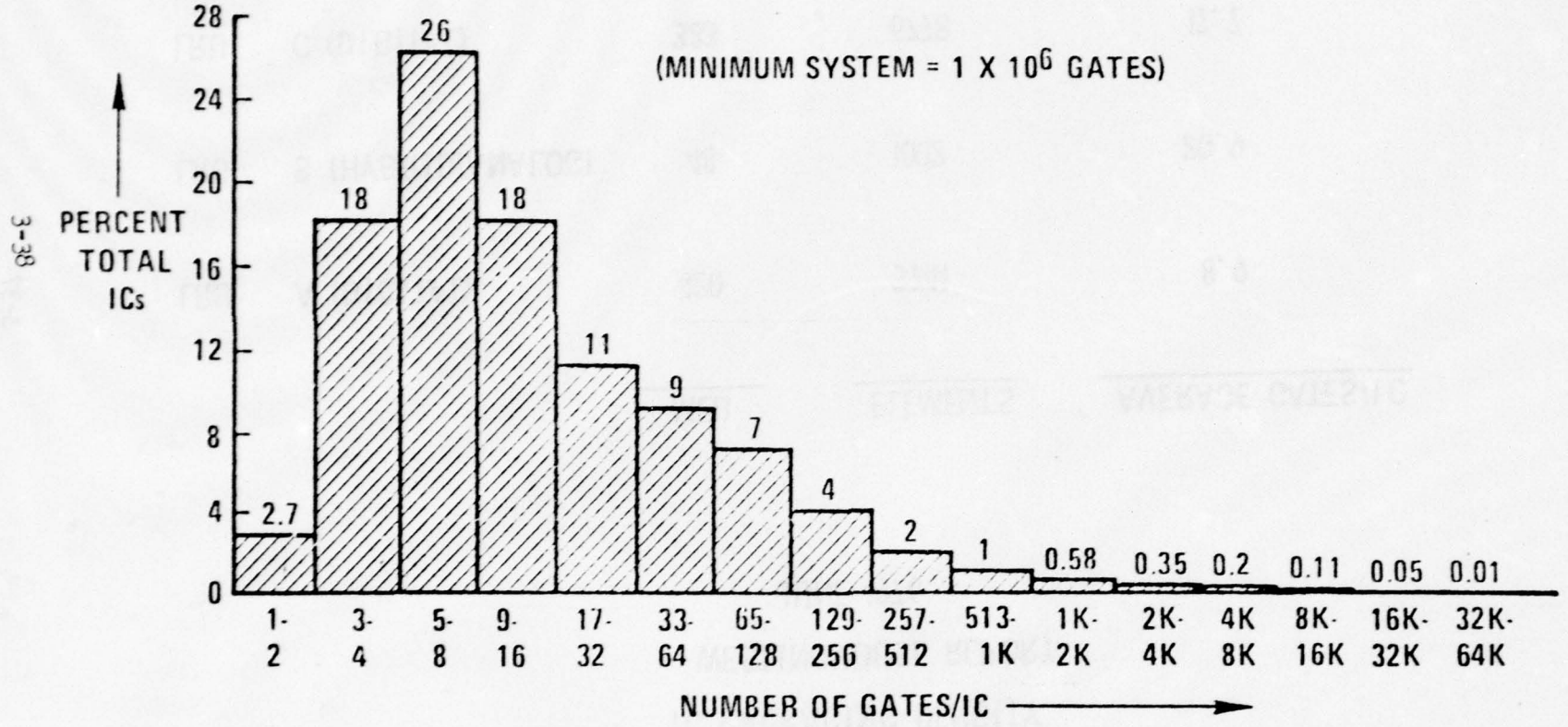
IC PACKAGING DENSITY

WESTINGHOUSE REPORT

JUNE 1976

	MED	ELEMENTS	AVERAGE GATES/IC
LRU A (DIGITAL)	420	3741	8.9
LRU B (HYBRID/ANALOG)	48	1002	20.9
LRU C (DIGITAL)	383	6778	17.7

ESTIMATE OF DISTRIBUTION OF ICs IN EQUIPMENT
STANDARD TTL - 1986



AVERAGE NUMBER OF GATES PER IC = 104

REFERENCE: EG&G REPORT

FIGURE 3.2-4

P7-1E

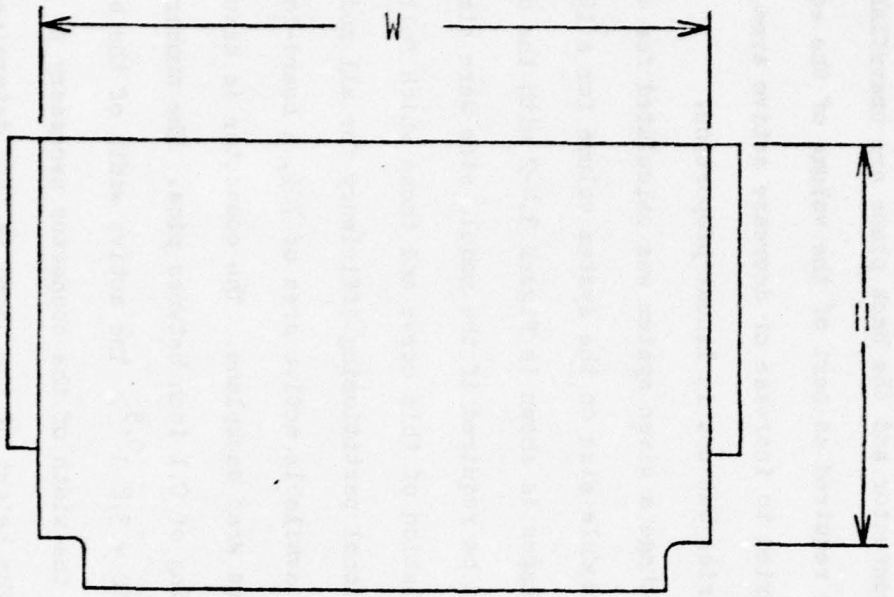
3.4 Weight and Volume Constraints

The effects of module size on the weight and volume of an avionic assembly are not discussed in sufficient detail in the reports to allow a valid analysis of those effects and a separate analysis was performed. For this purpose, a module was postulated as shown in Figure 3.4-1. The active area (W x H) is the space available for mounting of components. The other areas of the module such as the guide rails, the connector and the back plane are unavailable for mounting of components but are required as part of the volume of the equipment. As the size of the board is varied to increase or decrease active area, the overhead area required also varies but not in linear proportion.

The volume required to package a given system was calculated for various size modules. The effects of module size on the system volume for a 100,000 gate system using 14 pin DIP IC packages is shown in Figure 3.4-2 with the data normalized to that volume which would be required if the module size were similar to that of the SEM 1A. The calculation of this curve and those which follow is based upon an equivalent functional partitioning efficiency for all module sizes, a packaging utilization of the available active area of 70%, a board-to-board spacing of 0.3 inches and a wire wrap backplane. The connector is assumed to be a double row of pins with spacing of 0.1 inch between pins. The number of pins required is determined by: $PINS = 3.8\ G^{0.5}$. The active width of the board, W, is set for this calculation as the width of the connector necessary to provide the required number of pins. The height of the board is then determined by dividing the module active area by this width. The IC gate density has been assumed to be 17.8 gates/IC for present technology and 104 gates/IC for 1985. To simplify the calculations, the volume of the equipment housing walls, bottom and top, etc., have been neglected.

The calculations, as shown by Figure 3.4-2, indicate that a significant decrease (down to 75%) in volume can be achieved by increasing the module size

POSTULATED MODULE

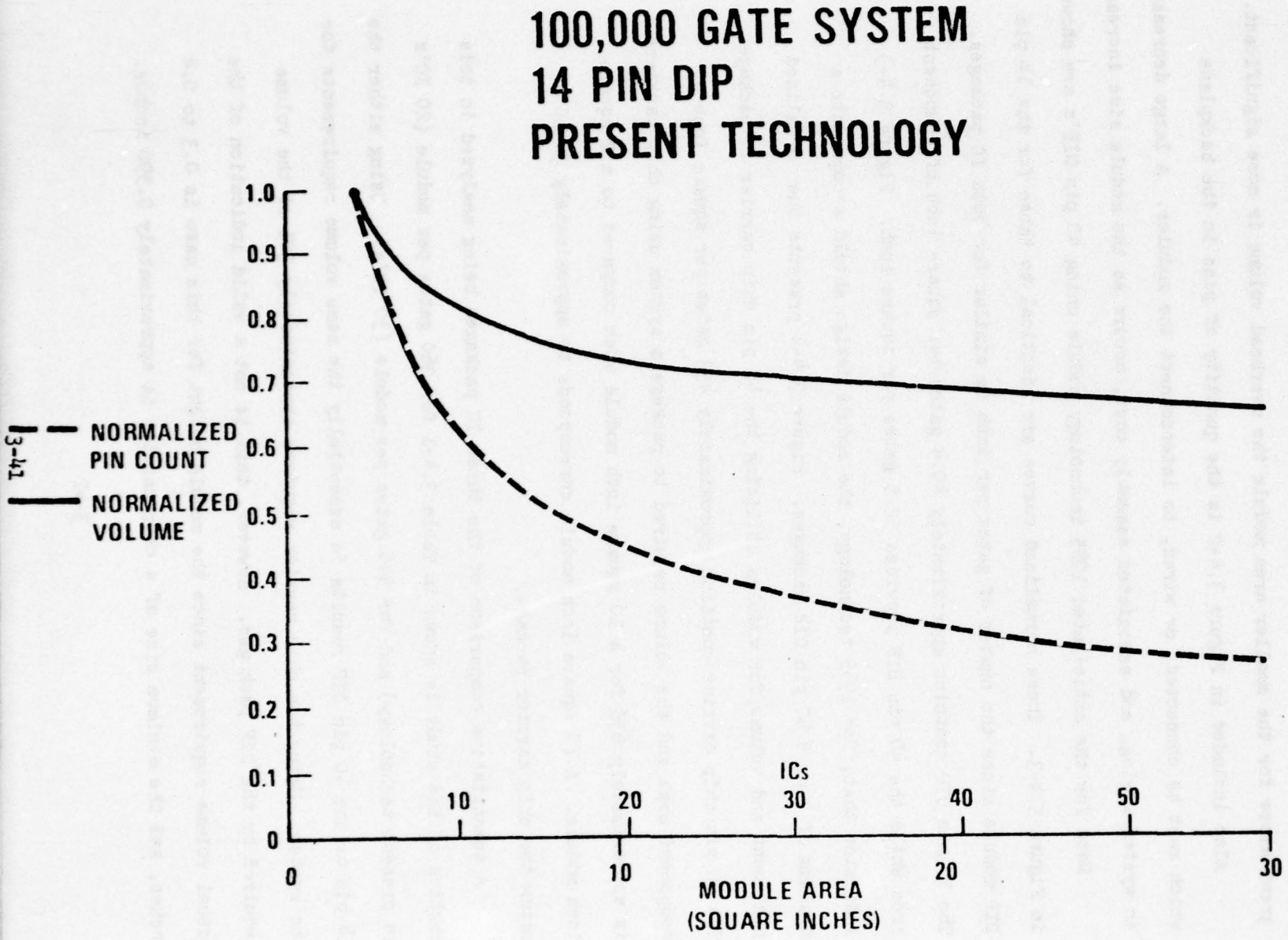


ACTIVE AREA = W X H

OVERHEAD AREA

- GUIDERAILS
- CONNECTORS
- BACK PLANE

FIGURE 3.4-1



P7-1655-17

FIGURE 3.4-2

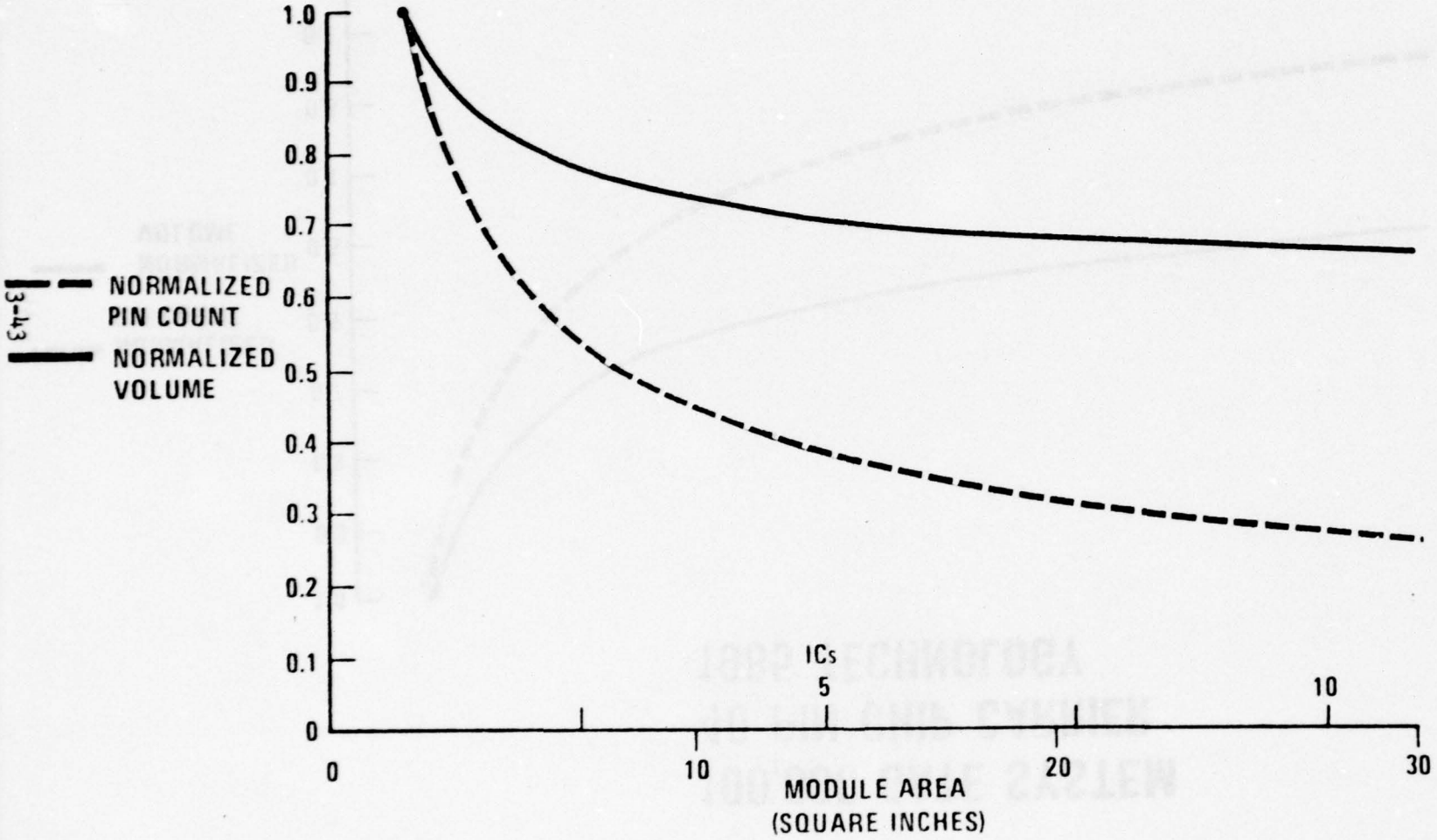
from 2 square inches (SEM 1A approximately) to 10 square inches or more. This is equivalent to a module assembled with 20-14 pin DIP IC's. The proportion of volume decrease as the module size increases above 10 square inches is not as great since for the smaller area module the overhead volume is more significant.

Also included in Figure 3.4-2 is the quantity of pins in the backplane which must be connected, or wired, to interconnect the modules. A large decrease in system wiring, and associated assembly cost, occurs as the module size increases.

Data for the anticipated 1985 technology module using 40 pin DIP's are shown in Figure 3.4-3. These normalized curves are identical to those for the 14 pin DIP module since the number of gates per inch is similar for both IC packages. The 14 pin DIP contains approximately 49.4 gates per square inch of component area while the 40 pin DIP provides 52.5 gates per square inch. Figure 3.4-3 indicates that, for 1985 technology, the module design should accommodate a minimum of 4 or 5 40 pin DIP packages. Figure 3.4-4 presents the ormalized pin count and volume for modules utilizing the 40 pin chip carrier IC package. The 40 pin chip carrier contains approximately 433 gates per square inch of component area and the volume required to package a system using chip carriers is approximately 63% for a 10 square inch module when compared to a 2 square inch module. A 10 square inch module corresponds to approximately 30 IC's using the chip carrier package.

A quantitative comparison of the three IC packages being analyzed in this portion of the study is shown in Table 3.4-1 for 360 gates per module (20 IC's in present technology) and for 540 gates per module (30 IC's). Using either the 14 pin or the 40 pin DIP results in essentially the same volume requirements for the system. Using the chip carrier requires approximately 30% of the volume required by the DIP packages. However, this is not a valid indication of the actual volume requirement since the module height for this case is 0.3 to 0.4 inches, and the minimum size of a chip carrier is approximately 0.590 inches.

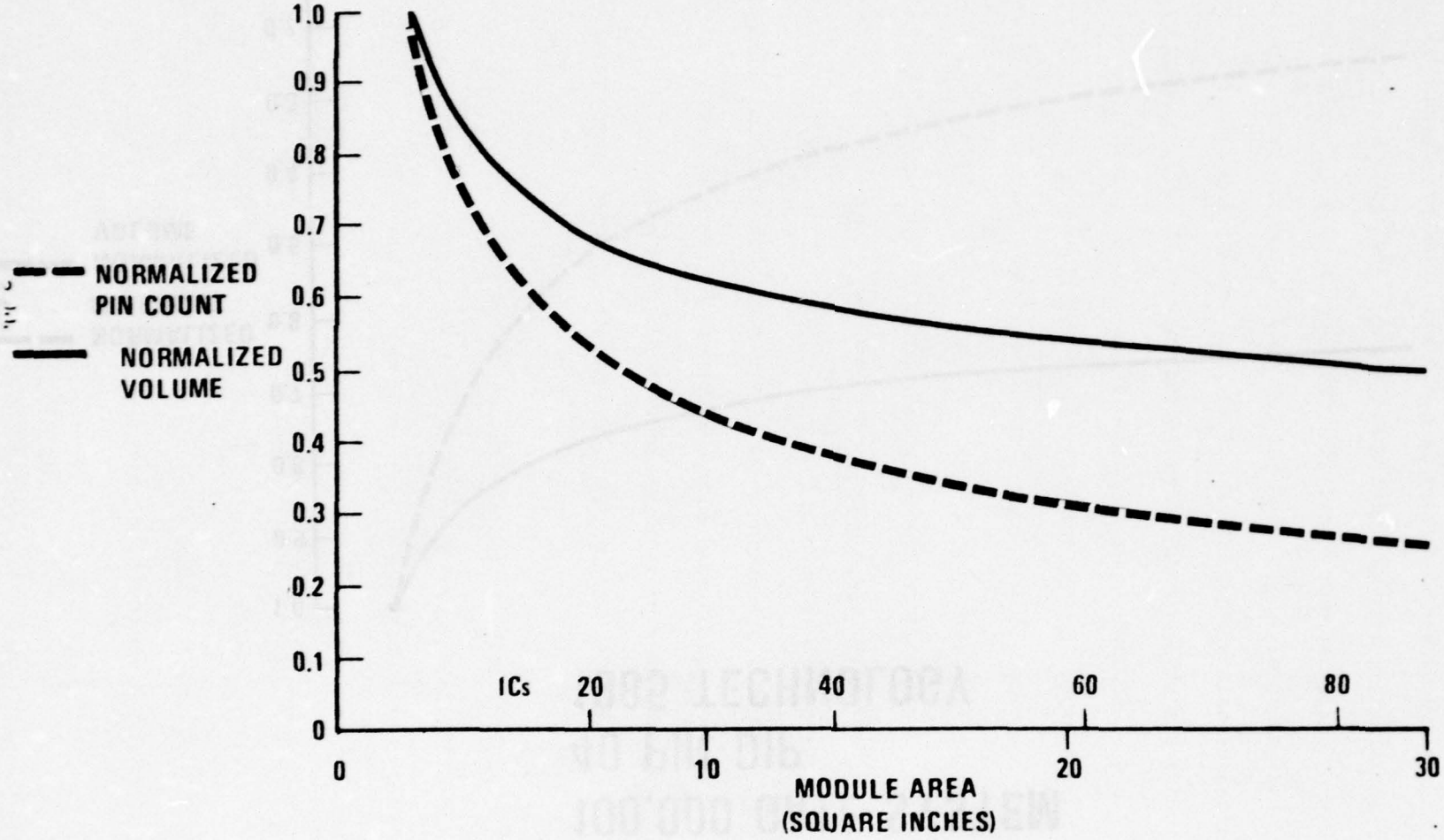
100,000 GATE SYSTEM
40 PIN DIP
1985 TECHNOLOGY



P7-1655-18

FIGURE 3.4-3

100,000 GATE SYSTEM
40 PIN CHIP CARRIER
1985 TECHNOLOGY



P7-1656-19

FIGURE 3.4-4

TABLE 3.4-1
PACKAGING COMPARISON
100,000 GATE SYSTEM

GATES/MOD	IC PACKAGE	SYSTEM VOLUME (CUBIC INCHES)	MODULE SIZE INCHES W	MODULE SIZE INCHES H	MODULE PINS	INTERCONNECT PIN COUNT
360	14 P DIP	1160	3.7	2.97	74	20000
	40 P DIP	1111		2.74		
	40 P LEADLESS	360		0.33*		
540	14 P DIP	1108	4.5	3.58	90	16352
	40 P DIP	1056		3.36		
	40 P LEADLESS	311		0.41*		

* INDICATED HEIGHT IS NOT CONSISTENT WITH CHIP CARRIER PHYSICAL DIMENSIONS

This unrealistic situation occurs since the calculations are based strictly upon the area of the IC footprint and do not consider the specific form factor. Increasing the module height to a more realistic value decreases the volume savings but can still result in a significant improvement.

To verify that this analysis is valid, quantitative data taken from the NAFI TR 2173 report has been compared to the generated curves. This comparison is shown in Figure 3.4-5 with the results of five partitioning studies on the Hughes Digital Scan Converter shown. The 5 different module sizes included are:

	CKT BD AREA (SQ. IN.)	ENCLOSURE HEIGHT (IN)	SPACE WIDTH (IN)	CONNECTOR PINS
SEM 1A	2.2	2.[illegible]	3.0	40
IMPROVED SEM (2A)	7.0	2.8[illegible]	6.64	100
CONCEPT 1 (Sized to be compatible with all ATR enclosures)	14.8	4.19	7.06	100
CONCEPT 6 (Sized to be compatible with 1/2 ATR enclosures)	18.0	4.78	7.62	165
HAC	29.8	7.35	3.0	100

The general trend of these data points follows the calculated curve, although the quantitative points fall below the calculated data. This can, in general terms, be explained. The calculations of this analysis were based upon utilization of the active area by components of 70%, but the actual utilization factors in the NAFI data are:

SEM 1A	70%
IMPROVED SEM	86.9%
CONCEPT 1	57.4%
CONCEPT 6	60.3%
HAC	80%

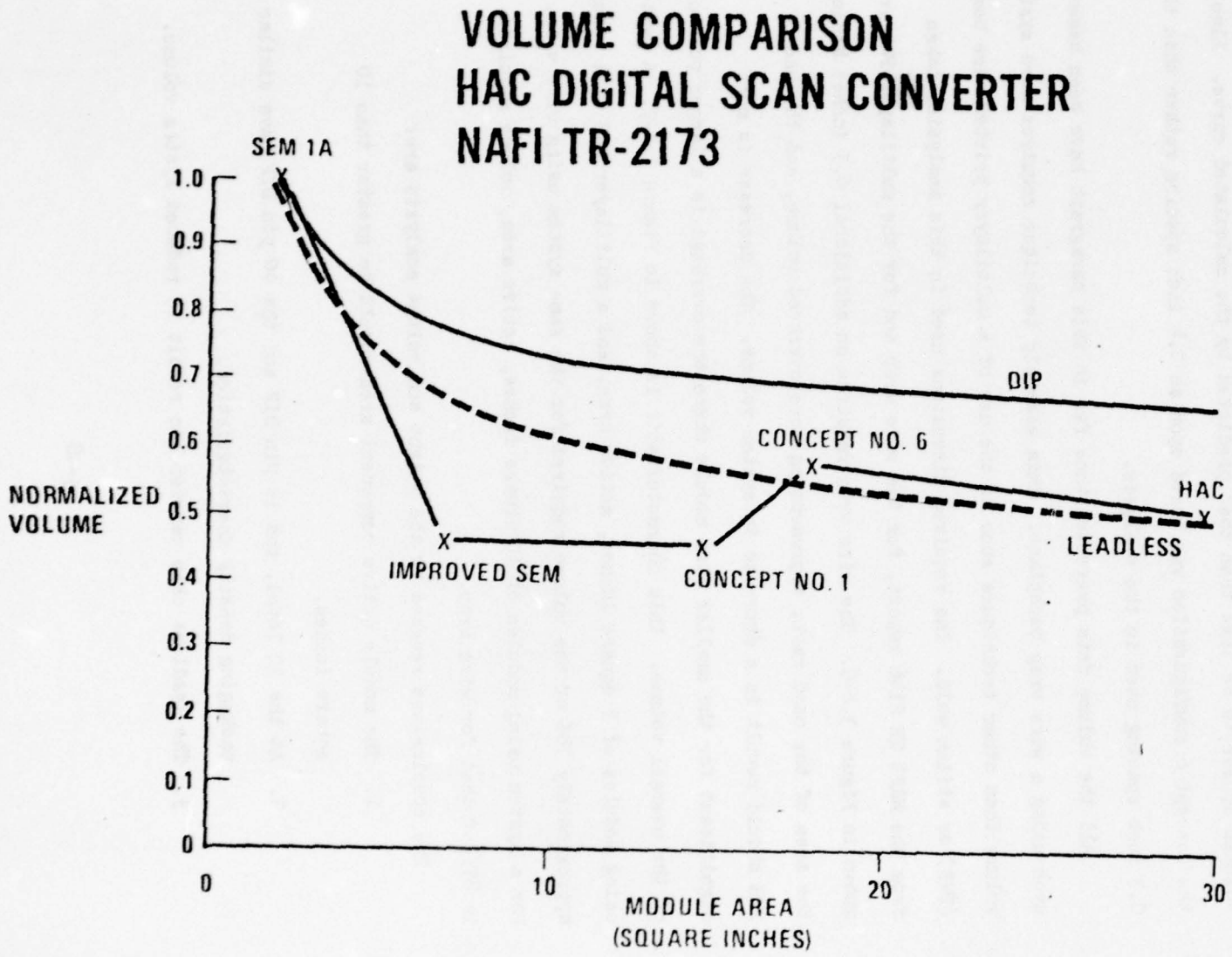

VOLUME COMPARISON
HAC DIGITAL SCAN CONVERTER
NAFI TR-2173
SEM 1A
DIP
CONCEPT NO. 6
HAC
LEADLESS
IMPROVED SEM
CONCEPT NO. 1
NORMALIZED VOLUME
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
10
20
30
MODULE AREA
(SQUARE INCHES)
P7-1655-20

FIGURE 3.4-5

The SEM 1A volume includes many unused functions since the partitioning was made using existing SEM modules. In the other cases the functional partitioning was more efficient and since the data are normalized to the SEM 1A, the normalized volumes appear to be less than that predicted by the calculated curve. Also, the Concept 6 configuration was based upon an 0.4 inch spacing rather than the 0.3 inch spacing used in the analysis.

All the volume data presented thus far in this paragraph have been based upon using a wire wrap backplane. This assembly technique requires more system volume than other techniques such as the use of a multilayer printed wire board (PWB) or stitch weld. The required dimensions used in this analysis, taken from the NAFI TR 2146 report, for the wire wrap and for the multilayer PWB are shown in Figure 3.4-6. The wire wrap requires an additional 0.5 inches behind the area of the card rack, representing more overhead volume, and the use of PWB should result in a decrease in system volume. The decrease is more significant for the smaller size module where the overhead is a larger portion of the overall volume. This characteristic is shown in Figure 3.4-7. A system using modules of 2 square inches, active area, and a multilayer PWB will require approximately 78% of the volume required for the same system using wire wrap. For a system using modules of 10 square inches, active area, volume required is 87% of that for wire wrap.

The conclusions reached by the weight and volume analysis are:

1. The module active component area should be greater than 10 square inches.
2. At the IC level, the 14 pin DIP and the 40 pin DIP have similar packaging density characteristics.
3. The leadless chip carrier can result in reduced system volume.

MODULE INTERCONNECTION -

BACKPLANE DIMENSIONAL REQUIREMENTS

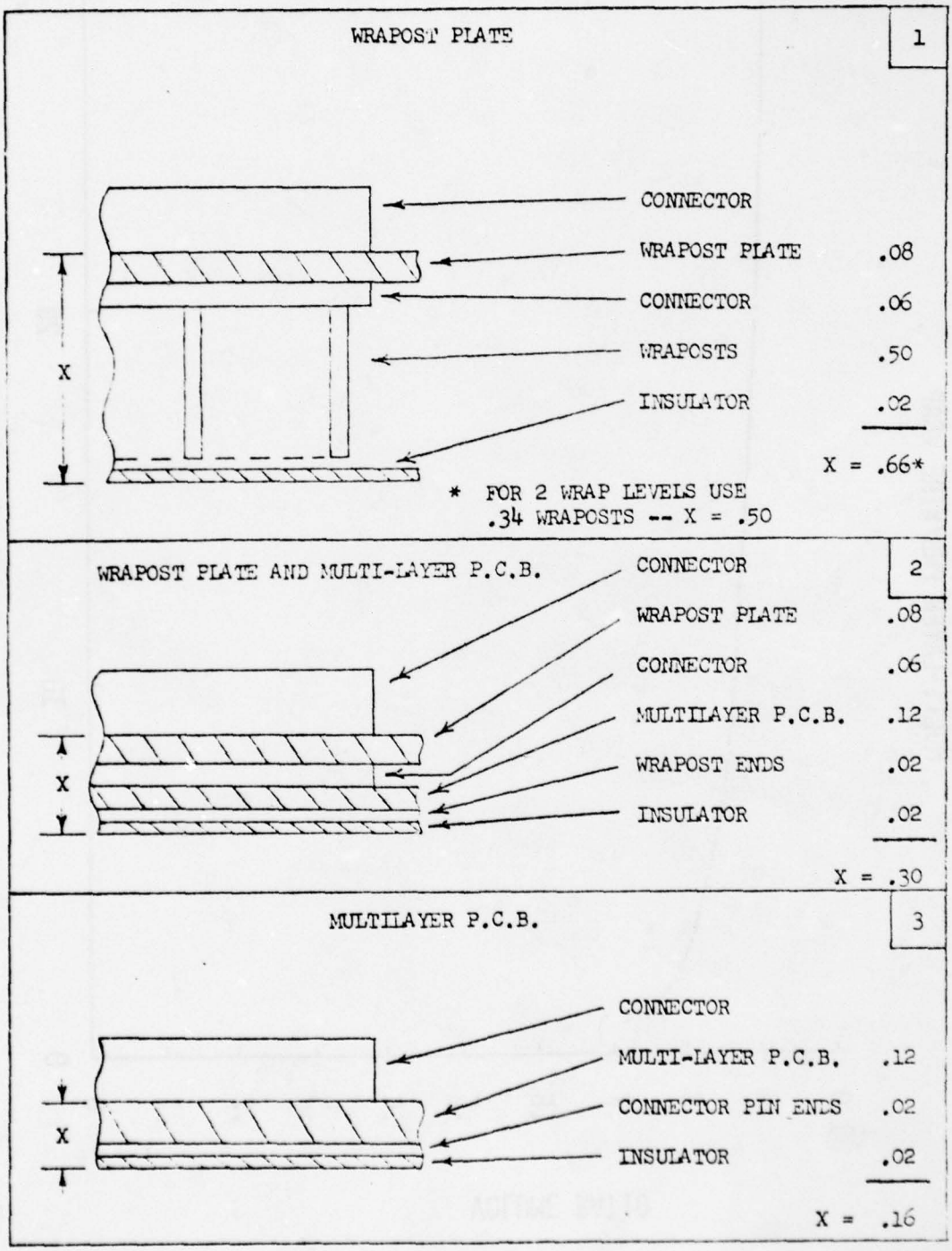


FIGURE 3.4-6

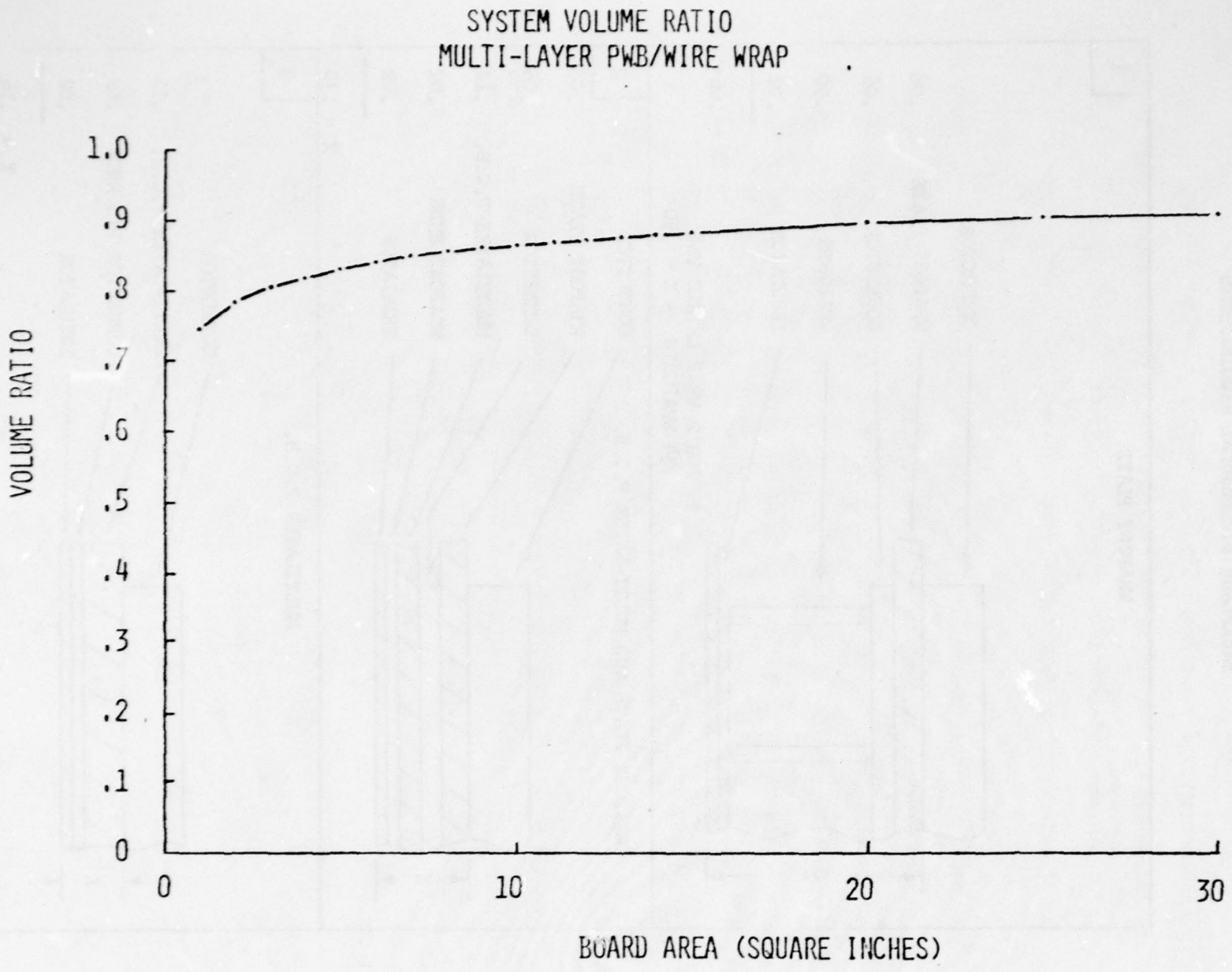

SYSTEM VOLUME RATIO
MULTI-LAYER PWB/WIRE WRAP
VOLUME RATIO
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
0
10
20
30
BOARD AREA (SQUARE INCHES)

FIGURE 3.4-7

3.5 Thermal Design Considerations

The power dissipation requirements for the module are determined by the number of IC's on the module and the power dissipation of each IC. Power dissipation in discrete components such as transistors, resistors, etc., is a special case and is not considered in this analysis but must be included when actual design decisions are being made for individual modules. The power dissipation of the individual IC is dependent, primarily, upon the technology used in manufacture of the component. There are numerous technologies in use at the present time and several others in research. Table 3.5-1 is a summary of the power dissipation characteristics for the more commonly used technologies. The power dissipation varies from 0.2 milliwatts per gate for I^2L logic to 30.0 milliwatts per gate for ECL. For the purpose of the thermal analysis, a power dissipation of 20 milliwatts/gate was selected. This selection is greater than or equal to all of the technologies considered except for ECL. Systems which use ECL, in general, require high speed logic which could be provided by Schottky TTL with less power dissipation. These systems are limited in number and will require special consideration.

The baseline reports describe various methods of cooling the modules. One method described is the use of the hollow-card module consisting of a heat exchanger of aluminum fin stock sandwiched between two PC Boards. Cooling air is forced through the fin stock dissipating the heat generated by the module. Assembly of this type of module is more costly and, in general, precludes the use of components requiring lead insertion through the board.

Cooling the module by conduction involves replacing the aluminum fin stock heat exchanger with a solid aluminum core or sheet. The heat is conducted through the multilayer board and the aluminum sheet to the structure side wall. The heat is transferred from the aluminum sheet to the structure by card guide-thermal clips.

In determining the method of heat dissipation which should be used for the standard module program, several factors were examined. Direct air flow across the module components under controlled conditions can provide the best method of heat dissipation. However, maintaining the controlled conditions required for satisfactory heat transfer is a complicated design problem especially if very close spacing of the modules is utilized, restricting the air flow path. With direct air cooling, smaller components placed behind larger components in the path of the air flow will be shielded resulting in a decrease in heat dissipation capability and localized hot spots. The effect on a single module design can change from one system to another depending upon the air flow characteristics within the individual racks or equipment housings.

In addition, the maintenance/troubleshooting of an avionic system will require, in general, the opening of the cabinets/racks and, possibly, drawers for access to the modules. This can disrupt the cooling air flow paths. By using conduction cooling, the heat dissipation paths can be more closely controlled and will not be adversely affected by the opening of cabinet doors, drawers, etc.

The standard module program must be based upon inter-system commonality to be economically feasible. This includes not only systems on an individual aircraft such as VSTOL/A but also commonality between future aircraft. Since not all of these aircraft will provide conditions amenable to convection cooling, the standard module design should be based upon total heat dissipation by conduction cooling. In those cases where cooling air can be provided, the thermal dissipation characteristics of the system will be improved resulting in lower IC junction temperatures and, thus, better component reliability.

Typical Power Dissipation Characteristics

TABLE 3.5-1

CIRCUIT TYPE	POWER/GATE (MILLIWATTS)
I^2L	0.20
NMOS	1.0
CMOS	1.0 (1 MHz)
LSTTL	2.0
TTL	10.0
STTL	19.0
ECL	30.0 (Unterminated)

The thermal conduction characteristics for a six inch by four inch glass epoxy board using an aluminum thermal plane was determined for several different board configurations. These detail calculations, presented in Appendix A for reference, indicate that the thermal dissipation requirements for a module can be satisfied within the physical size limitations set by the number of integrated circuits when DIP components are used. A summary of the total power dissipation requirements and capabilities for three configurations using DIP components is shown in Table 3.5-2. In all cases the power dissipation capability exceeds the required power dissipation.

The thermal dissipation characteristics of a module utilizing a ceramic substrate bonded to an aluminum frame are presented in Appendix B which describes a configuration of the standard module for chip carrier installation. This module is capable of dissipating approximately 18.3 watts which exceeds, by 2.5 watts, the power dissipation capability of the glass epoxy board.

Power Dissipation Requirements and Capability

TABLE 3.5-2

IC's	PINS/IC	Gates/IC	Total Gates	MW/Gate	Total Power Dissipation Required (watts)	Power Dissipation Capability (watts)
30	16	17.8	534	20	10.68	10.96
12	24	40	480	20	9.60	12.6
6	40	100	600	20	12.00	13.35

3.6 Built-In-Test Concept

In a standard module program, the built-in-test (BIT) concept to be utilized in the system development and in the modules used in those systems must be established very early in the program to be effective. The overall system philosophy on BIT monitoring and fault isolation requirements must be established prior to any design effort on individual modules. The purpose of BIT, at the system level, is to increase operational readiness by reducing system down time by providing quick, straightforward failure identification, fault isolation and repair capabilities. These capabilities can be provided by incorporating BIT system performance monitoring, malfunction reporting, and fault isolation to the module level as an integral part of the system design.

To obtain maximum benefits from BIT, it is necessary that all replaceable sub-assemblies within a system are tested at some level of BIT.[13] The overall performance of a system or subsystem is monitored with end-to-end BIT with stimuli applied to inputs and the output responses measured. This can be done with the system off-line or with the system on-line. On-line monitoring can be achieved by monitoring normal input and output signals and comparing with known system transfer characteristics or by time sharing the input between normal and test signals. By proper selection of input stimuli, it is usually possible to isolate the fault to a functional block within the system. Further BIT testing at the subsystem level is then necessary if the isolated functional block is not a single replaceable assembly. At the system level, the desired BIT capability can be provided in the hardware design or in the software programs. There are advantages to each approach and each requires consideration in the initial design of a system. It is anticipated that systems using SAM will provide both types of BIT to some degree.

There are several design features to be considered when designing BIT into the hardware. These are:

(1) The reliability of the hardware required to perform BIT should exceed that of the hardware being tested. If this is not the case, the probability of failure in the BIT circuit may be as great or greater than the probability of failure in the circuit under test. This could result in expending as much maintenance time and cost for repair of BIT hardware as for operational hardware.

(2) A failure in the BIT hardware should not affect performance of the system.

(3) The BIT circuitry should be kept as simple as possible but must be sufficiently effective.

(4) The circuit used for BIT should be of the same type used in the operational circuits and use the same component types.

(5) Fault indicators such as light emitting diode (LED), incandescent or neon lamps should be provided where possible at the replaceable sub-assembly level to provide continuous visual monitoring of system performance.

Performing BIT with software also impacts the hardware and must be considered in the design. Some of the hardware provisions which might be necessary are:

(1) Isolation must be provided between normal inputs and test inputs.

(2) Decision circuits which monitor output data must provide adequate tolerance.

(3) Test input signals should be provided which closely simulate actual inputs.

(4) Existing data transmission systems should be used where possible.

(5) Optimize fault isolation by judicious selection of monitor points.

(6) The probable increase in computer size to accommodate the BIT capabilities must be included in the initial design of the system.

The quantitative impact of providing BIT, whether it is provided totally in hardware or in the software, on the design of a standard module is difficult to predict. Discussions with various design personnel indicate that BIT requires a hardware increase on the order of 10 to 25%. The Built-In-Test (BIT)

Design Guide[13] does not provide any further insight except that in one example for a transmitter it is stated "... to provide a thorough test of 95% of all components in the normal transmitter fault logic would amount to an increase of about 25% in overall cost, space and complexity."

The only other quantitative data available in the Data Base and Reference reports is found in the G.E. report[7] which provides detail mechanical layouts, block diagrams and estimated parts lists of three power supplies for the Advanced Integrated Display System (AIDS) Program. In each case the hardware required to perform BIT is identified. The portion of the total hardware identified for BIT is:

	BIT Complexity	
Assembly	Component Count	Area
Low Voltage Power Supply	26%	14.3%
High Voltage Power Supply	20%	16.7%
16 KV Power Supply	20%	16.7%

Based upon the data available it is concluded that BIT will require an additional 15 to 25% of overall system area. This increase may be at the system level by the addition of modules specifically to perform BIT or by an increase in the complexity of each module circuit. The overall system BIT philosophy will determine which of these approaches, if not a combination of both, will be taken. It must be noted, however, that failure to adequately define a system BIT philosophy prior to the design of individual modules could, and probably will, result in module designs which are totally incompatible with the later defined system BIT requirements. This condition will create an inefficient and more costly maintenance program than could be otherwise achieved.

3.7 Reliability

As discussed previously, the two primary cost areas in the life of an avionic system are the initial acquisition cost and the follow-on support costs. The reliability of the components, as well as the number of components on a module, affects both of these cost areas since the initial cost of high reliability components is, in general, higher than for standard military grade; and since component reliability significantly affects the life cycle spares cost which is a major portion of system support costs. An analysis of the effect upon life cycle spares cost is documented in the NAFI TR2146 report and is summarized in the following paragraphs.

A model for the flow of spare modules was developed as shown in Figure 3.7-1. The model assumes these are N_E equipments which receive good modules from each base and there are M bases supplied by a single depot. The depot obtains modules from one or more factories. Both the depot and the bases are assumed to have only sufficient spares to assure a given probability of meeting the spares requirement during the replenishment time. The replenishment time for a depot, t_{DF}, is assumed to be 6 months and for a base, t_{DD}, it is 1 month. New modules from the factories flow to the equipments through the depot and the bases. Modules which are removed from equipment are routed to the depot through a base for test. Modules which test good at the depot are returned to base with a depot delay time of t_T plus twice the depot to base delay time t_{DD}. Modules which test bad are discarded at the depot for the purposes of this analysis. All modules are assumed to have the same number of integrated circuits with the same cost and reliability.

The mathematical model used is given by:

$$\frac{R}{N_{IC}} = (1+K_L)K_{OC}^{\lambda_{IC}} \left[(1+2K_{GB})t_{DD} + K_{GB}\, t_T + t_{DF} + t_L \right]$$

$$+ E_x \sqrt{\frac{N_T}{N_E N_D}\, (1+1K_L)K_{OC}^{\lambda_{IC}}} \left[\sqrt{(1+2K_{GB})t_{DD} + K_{GB}\, t_T} + \sqrt{\frac{t_{DF}}{M}} \right]$$

The values and definitions of the variables used in this analysis are shown in Table 3.7-1.

The ratio of spares per module, R, during the life cycle of all systems is assumed to be 0.1, i.e. life cycle spare costs is 10% of system operating module acquisition cost. Ten percent was used since this is approximately the border line between a relatively insignificant cost and a significant cost. It was also justified on the basis that spares cost needs to be less than the thirty percent which has been achieved and considered excessive in some instances. Another rationale for the ten percent choice is that the spare life cycle cost is approximately proportional to failure rates and, since failure rates have relatively large standard deviations a nominal R ratio greater than 0.1 could have disasterous life cycle cost impact for modules in the upper range of the failure rate distribution curve.

The Heads-Up Display (HUD) of the F-15 aircraft was used to estimate the values of some of the variables to be used in the model. The failure rates were both actual and predicted values. This hypothetical system case was analyzed with the failure rate of the integrated circuits as a variable to find the number of integrated circuits per module which would cause the ratio of spares per module to be 0.1.

The maximum number of integrated circuits per module, N_{IC}, to provide an 0.98 probability of adequate spares while maintaining an 0.1 lifecycle spare cost ratio is shown in Figure 3.7-2. Using the predicted failure rate of 9.5×10^{-7} failures per hour derived from the F-15 HUD field data, the maximum number of 14-16 pin IC's allowed per module is 8.

Based upon the conclusions drawn from other areas of this study, the primary area of interest for the SAM program is between 0 and 50 IC's per module and this area of the curve is shown in more detail in Figure 3.7-3. Note that the axes have been changed from Figure 3.7-2. It can be seen from

SPARE MODULE FLOW

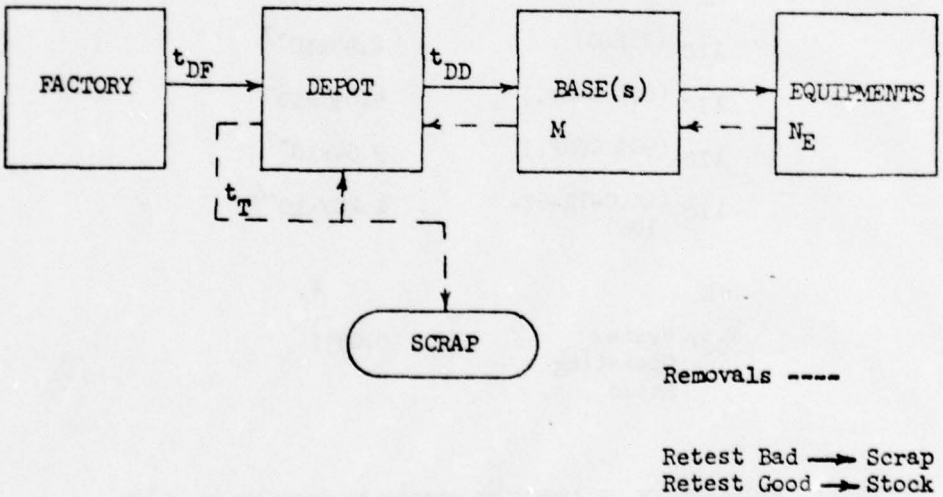


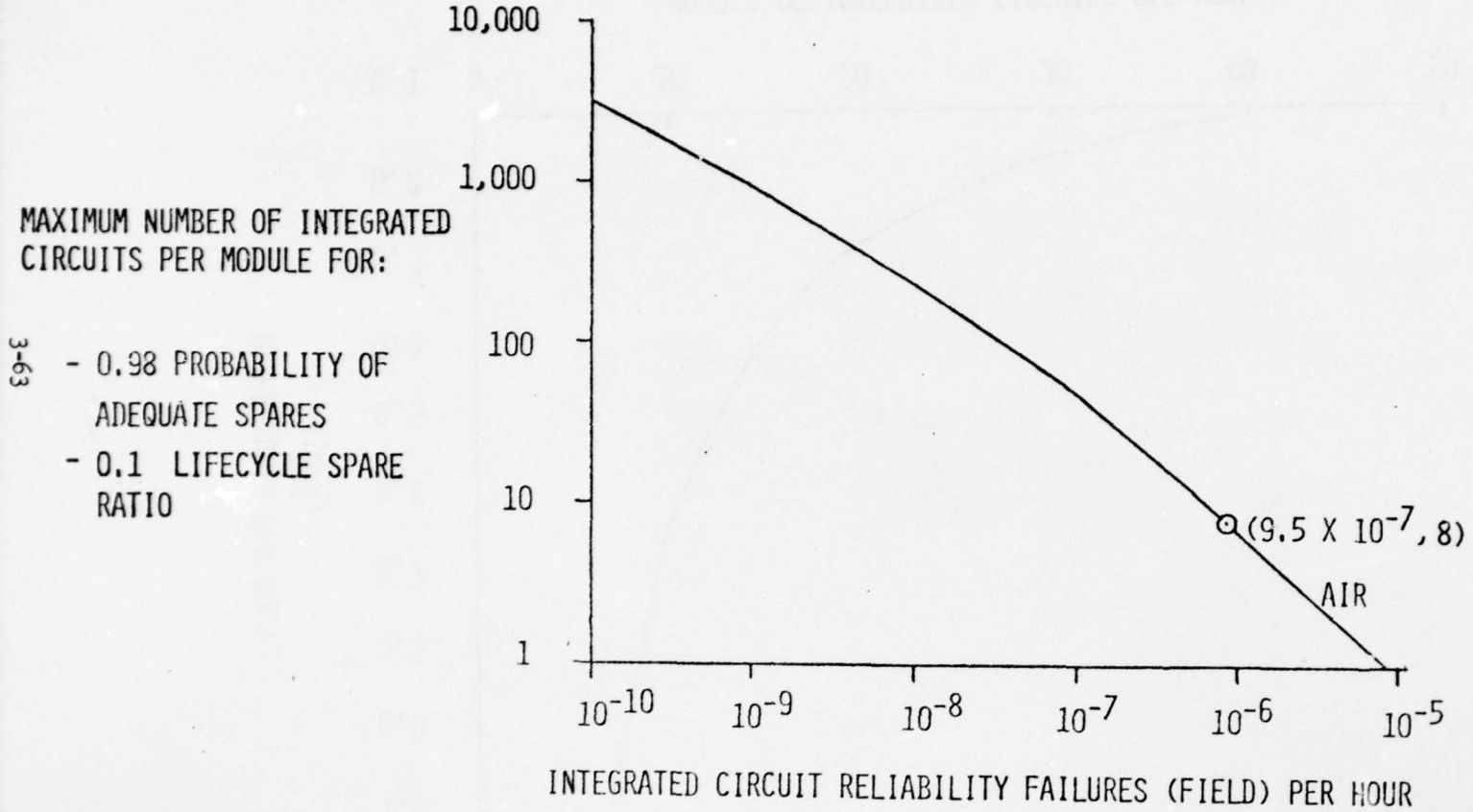
FIGURE 3.7-1

SPARE MODULE FLOW ANALYSIS VARIABLES

VARIABLE	VALUE
t_L, System Life	87,600.
t_{DD}, Depot Delay	720.
t_T, Test Delay	168.
t_{DF}, Factory Delay	4,000.
K_L, Induced Failures	1
N_E, No. Equip.	20
M, No. Bases	2
N_D, IC's/Equip.	752
N_T, No. Types	20.
R, Spare Ratio	0.1
K_{GB}, Retest Good	0.5
λIC (FIELD)	2.45×10^{-7}
λIC (60% CONF.)	4.895×10^{-7}
λIC (90% CONF.)	9.54×10^{-7}
λIC (RADC-TR-67-108)	1.287×10^{-6}
πE	4.
K_{OC}, System Operating Ratio	0.0571

NOTE: PROBABILITY OF ADEQUATE SPARES ASSUMED TO BE 0.98

Table 3.7-1



REF: NAFI TR 2146

FIGURE 3.7-2

FIGURE 3.4-6

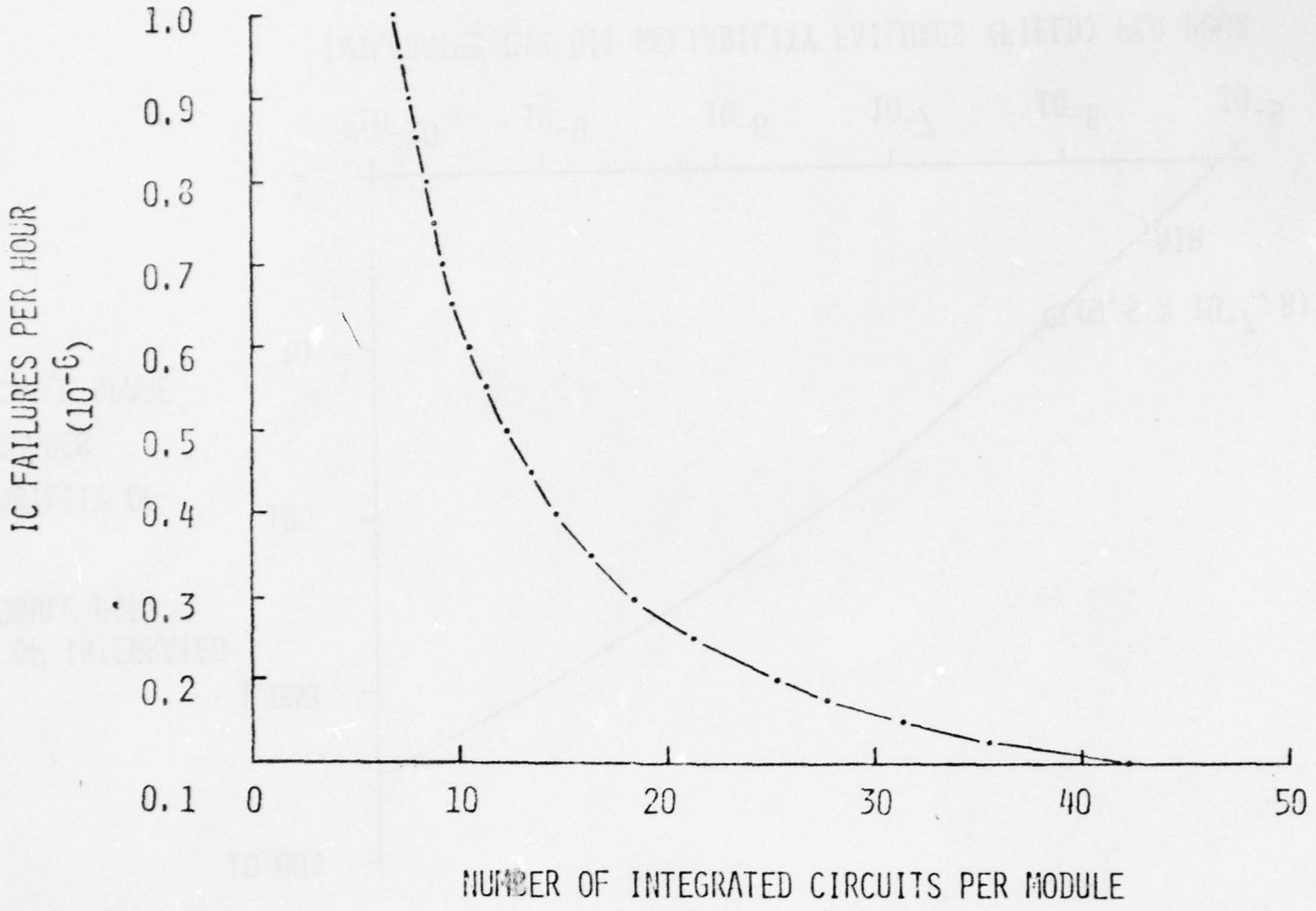

1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
IC FAILURES PER HOUR
(10^{-6})
0
10
20
30
40
50
NUMBER OF INTEGRATED CIRCUITS PER MODULE

FIGURE 3.7-3

this figure that the allowed number of IC's per module is very sensitive to changes in IC failure rate in the area of interest, 20 to 30 IC's.

To determine if the F-15 HUD failure rate data are what might be expected from a new avionic program, failure rates were calculated using MIL-HDBK-217B as a guide. These calculated failure rates, based upon MIL-M-38510 class B components, a maximum 105° C junction temperature and an uninhabited, airborne environment are shown in Table 3.7-2. Using these failure rates, the standard module can contain 27 14-16 pin integrated circuits using TTL technology or 9 14-16 pin integrated circuits using ECL technology. The same analysis for 1985 indicates a maximum of 13 40 pin IC's using TTL or 3 40 pin IC's using ECL is acceptable. It should be noted that if the junction temperatures are maintained at a lower maximum, thereby improving the component failure rates, the allowable number of IC's will increase. For instance, for a maximum junction temperature of 85°C, the allowable number of 14-16 pin IC's using TTL logic is approximately 30.

TABLE 3.7-2

INTEGRATED CIRCUIT PREDICTED FAILURE RATES

0.98 PROBABILITY OF ADEQUATE SPARES

0.1 LIFECYCLE SPARE COST RATIO

MIL-HDBK-217B FAILURE RATES

- MIL-M-38510, CLASS B COMPONENTS
- 105°C MAX JUNCTION TEMPERATURE
- AIRBORNE, UNINHABITED

GATES/IC	TECHNOLOGY	FAILURE RATE (10^{-7})	IC/MODULE BASED ON SPARES ANALYSIS
17.8	TTL	1.81	27
	ECL	6.96	9
104	TTL	4.25	13
	ECL	22.5	3

4.0 MODULE CONFIGURATION DEVELOPMENT

Each of the factors which affect module size has been discussed in the previous paragraphs. The conclusions reached from the analysis of each individual factor are summarized as follows:

Functional Commonality - The packaging concept should provide for a maximum of 30 IC's per module to achieve any savings in total ownership cost.

Connector - The number of pins required to electrically interface the module into the system can be estimated by the relationship;

$$PINS = 3.8\ G^{r},$$

where $0.58 > r > 0.52$

The connector type should be the NAFI blade and fork with 0.1 inch pin spacing.

Integrated Circuit Packaging Technology - Present technology is 14-16 pin IC with an average of approximately 18 gates per IC. The 1985 technology is projected to be a 40 pin IC with an average of approximately 100 gates per IC. The dual-in-line package will be more widely used than flatpacks. The chip carrier package can provide a higher gate density package.

Weight and Volume Constraints - The module active area should be greater than 10 square inches (more than 20 dual-in-line IC's) to minimize effect of overhead volume.

Thermal Considerations - Thermal conduction requirements can be satisfied within size limitations set by IC count using DIP packaging.

Built-In-Test - The inclusion of BIT increases the complexity and size of a system by 15 to 25%.

Reliability - The module should contain 27 or less 14-16 pin IC's using TTL logic with maximum junction temperatures of 105° C. With junction temperatures of 85° C, the maximum number of 14-16 pin IC's can be increased to 30.

The exact number of integrated circuits which should be contained on a standard module is not apparent from these conclusions. However, a range of optimum integrated circuit component capability is clearly indicated. The standard module size is optimized if it provides for between 20 and 30 integrated circuits. To provide further visibility into the selection of a specific number within the range, the estimated IC count for postulated standard functions from the reports was compiled. This compilation is provided in Figure 4.0-1 showing the number of standard function modules which require a specific number of IC's. These data indicate that of the 89 standard or common functions identified, 49 require 30 IC's or less with 7 requiring exactly 30. This indicates that, from a functional partitioning standpoint, the module should be designed to accommodate a number of IC's in the upper end of the optimum range. For this reason, a capability of 30 IC's has been selected for the standard module.

For 30 IC's per module and using present technology of 18 gates per IC, the standard module will contain 540 gates. This corresponds to 5-40 pin IC's of approximately 100 gates each using 1985 projected technology. Using the relationship, $PINS = 3.8\ G^{0.52}$, the number of required pins in the interface connector is estimated to be 100. The physical layout of a board, 6.0 inches by 4.0 inches, with these characteristics and containing 30-16 pin dual-in-line packages is shown in Figure 4.0-2. Assuming 17.8 gates per DIP and 20 milliwatts per gate, the board thermal dissipation requirement is 10.68 watts. Figure 4.0-3 is a physical layout for 12-24 pin DIP's. Assuming 40 gates per DIP and 20 milliwatts per gate, the board thermal dissipation requirement is

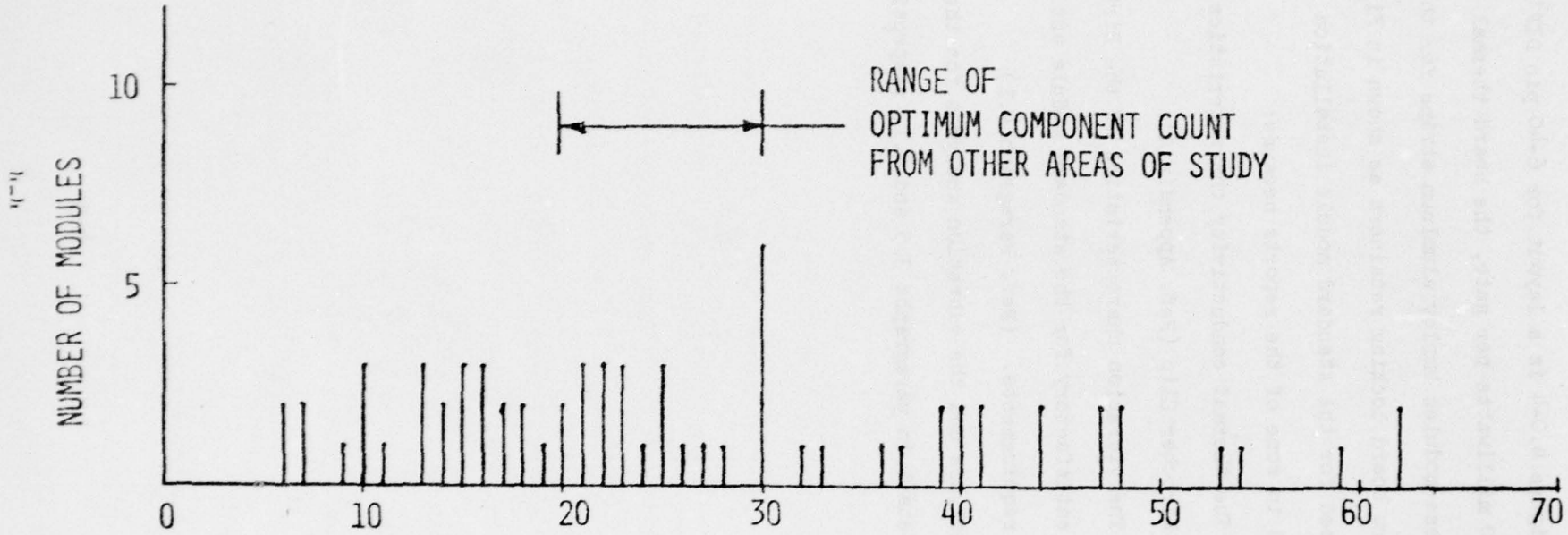
9.6 watts. Figure 4.0-4 is a layout for 6-40 pin DIP's. Assuming 100 gates per DIP and 20 milliwatts per gate, the board thermal dissipation requirement is 12 watts. These modules employ aluminum strips for thermal conduction to the side walls thru board locking retainers as shown in Figure 4.0-5. The locking retainer is used for the standard module installation instead of the Birtcher Clip described in some of the reports because:

1. The thermal conductivity characteristics are marginal for the Birtcher Clip (Ref. Appendix A).
2. The vibration characteristics of the Birtcher Clip are not satisfactory for the standard module anticipated vibration requirements. (Ref. Paragraph 4.1)

The thermal analysis and the vibration analysis for the recommended module are discussed in detail in paragraphs 3.5 and 4.1, respectively.

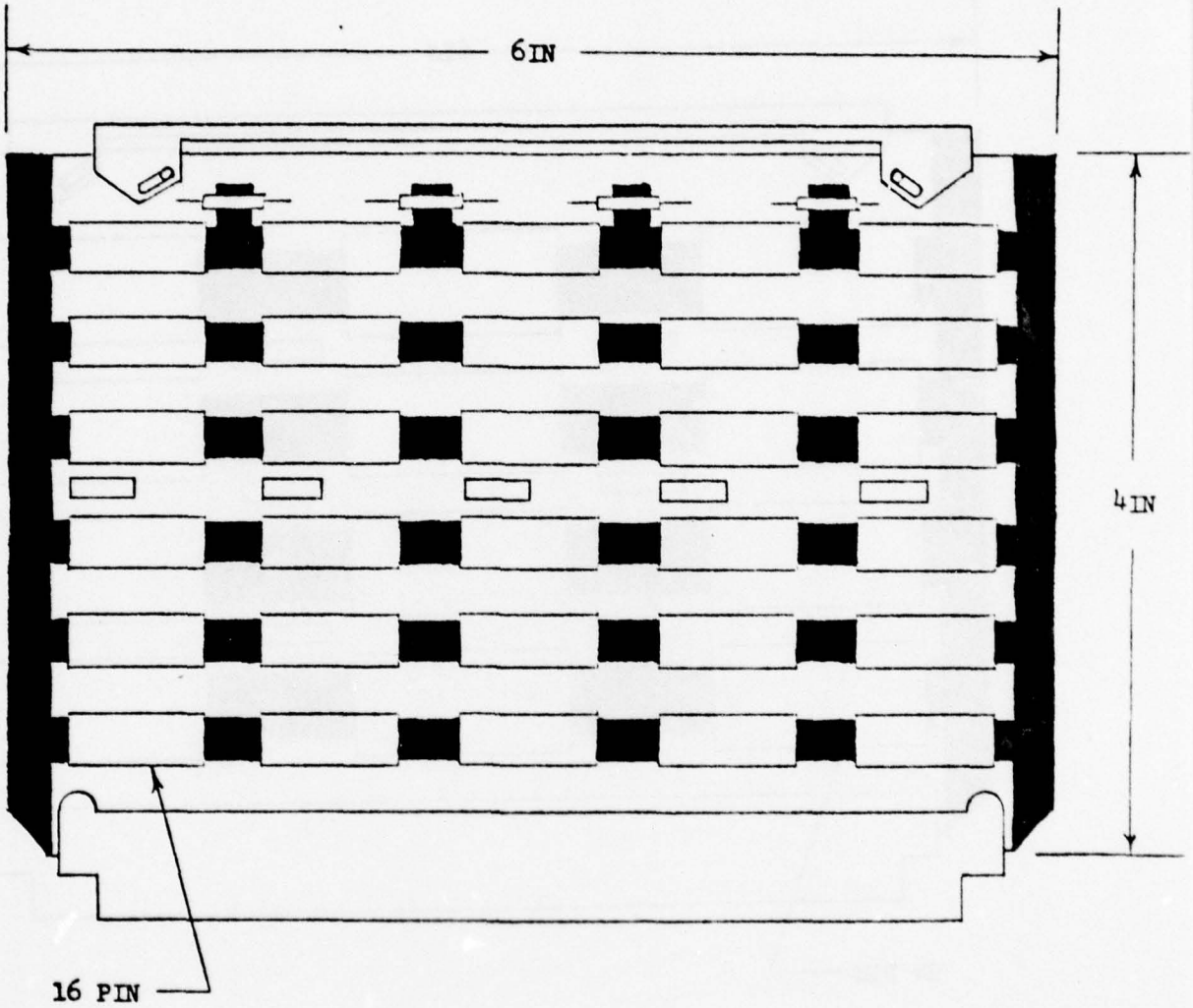
FUNCTIONAL PARTITIONING
ESTIMATED IC COUNT

REF: RAYTHEON
NAFI TR 2173
HONEYWELL
WESTINGHOUSE



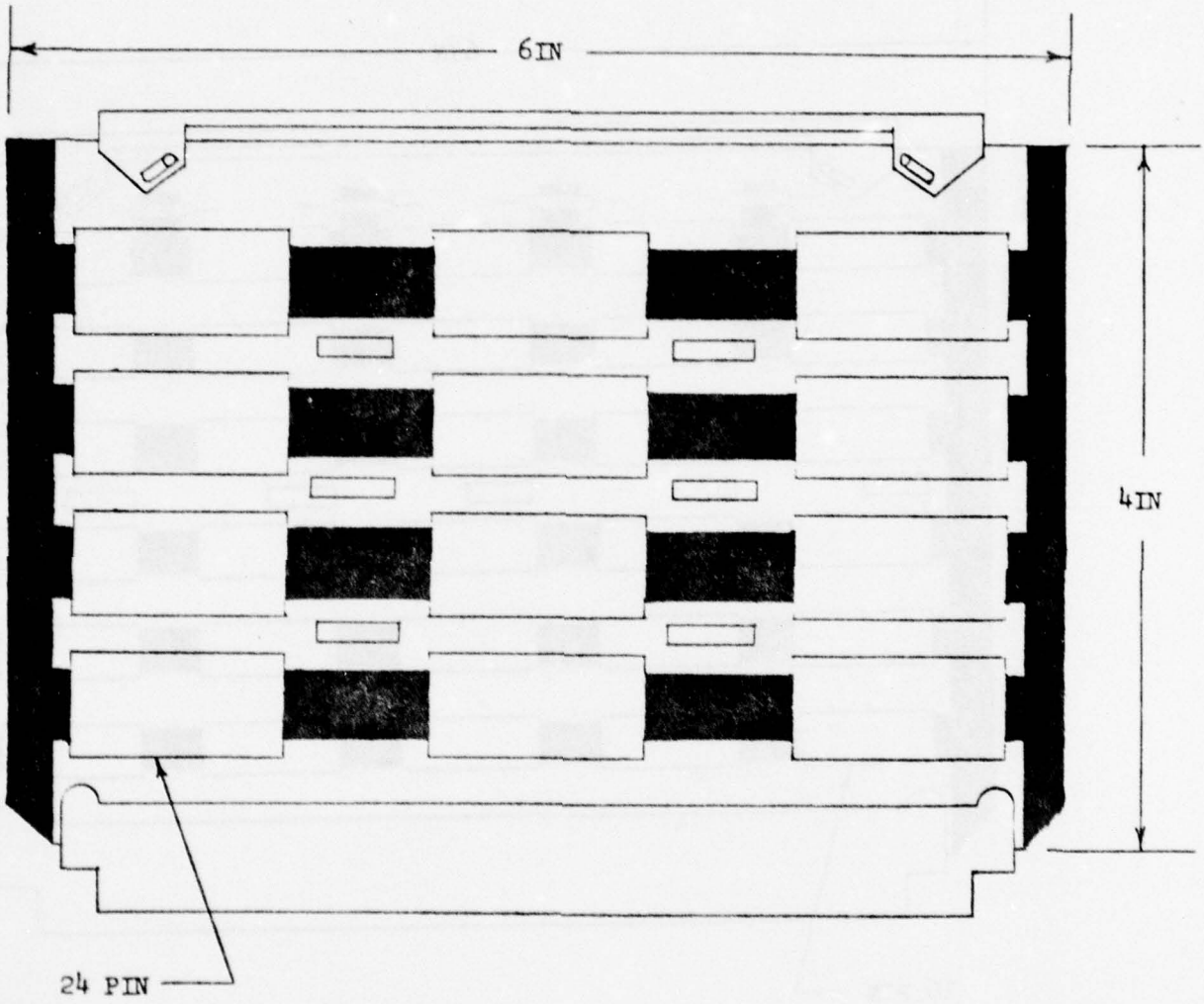
IC PER FUNCTIONAL MODULE
STANDARD OR COMMON FUNCTIONS

FIGURE 4.0-1



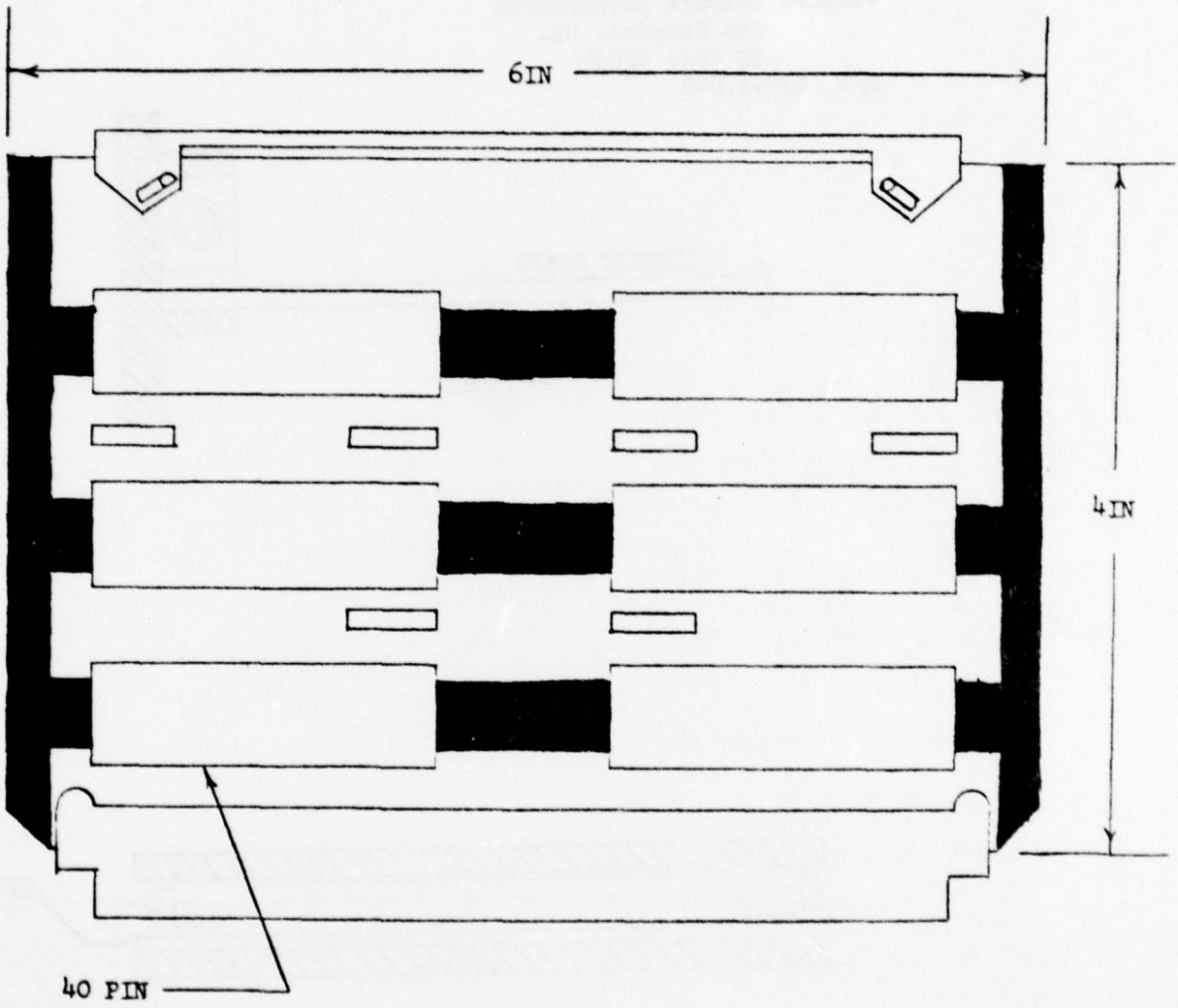
THIRTY DUAL IN-LINE PACKAGE INSTALLATION
POWER DISSIPATION - 10.68 WATTS

FIGURE 4.0-2



TWELVE DUAL IN-LINE PACKAGE INSTALLATION
POWER DISSIPATION - 9.6 WATTS

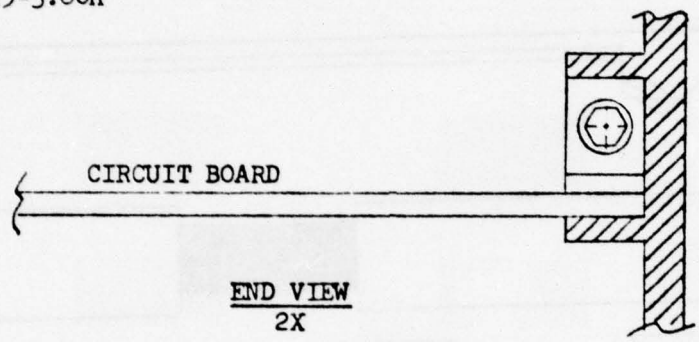
FIGURE 4.0-3



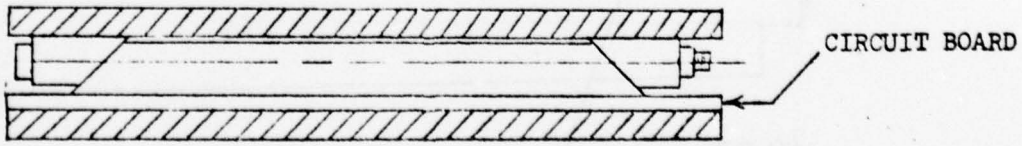
SIX DUAL IN-LINE PACKAGE INSTALLATION
POWER DISSIPATION - 12 WATTS

FIGURE 4.0-4

"Card-Lok" Retainer
Vendor: Calmark Corporation
San Gabriel, Ca.
ID Code 52094
P/N: 225-3.80H



END VIEW
2X



SIDE VIEW
1X

LOCKING RETAINER INSTALLATION

FIGURE 4.0-5

4.1 Vibration Design

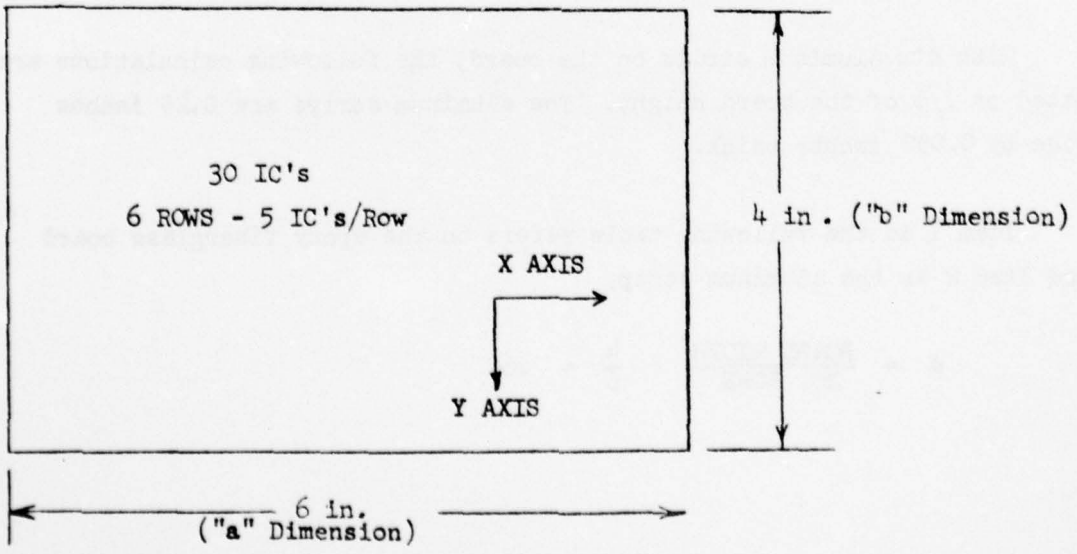
Initial plans were to use Birtcher 24S PCB Lok-Tainer clips for module edge support. Test data from programs conducted on other black boxes with cards using Birtcher clips have shown that the clips have very poor vibration response characteristics. The following calculations indicate an unacceptable fundamental resonant frequency of the module using the Birtcher clips and show that by replacing the clips with locking retainers, the fundamental resonant frequency can be increased to an acceptable level.

4.1.1 Birtcher Clip Analysis

The fundamental resonant frequency of a 6 in. x 4 in. x .062 in. epoxy fiberglas board, using Birtcher 24S PCB Lok-Tainer clips for card retention is determined as follows.[19] The weight of the board must first be determined to calculate the natural frequency and the deflection.

FIGURE 4.1.1-1

Vibration Model



CIRCUIT BOARD WEIGHT CALCULATIONS

CIRCUIT BOARD $6 \times 4 \times .062 = 1.488 \text{ in}^3$

$1.488 \text{ in}^3 \times .066 \text{ Lb/in}^3 = .098 \text{ lb} = 1.571 \text{ oz}$

IC's $30 \times 1.1474 \text{ Gram/IC} = 34.42 \text{ Grams} = 1.214 \text{ oz}$

ALUMINUM STRIPS $6 \times 5.5 + 2 \times 4 = 41 \text{ in.}$

$41 \times .25 \times .05 = .51 \text{ in}^3 = .051 \text{ Lb.} = .816 \text{ oz}$

(Six strips across board + one strip on each edge)

HANDLE .183 oz.

CONFORMAL COATING .112 oz.

TOTAL VIBRATING WEIGHT $1.571 + 1.214 + .816 + .183 + .112 = 3.895 \text{ oz} = .243 \text{ Lb.}$

Assuming mass is evenly distributed to simplify calculations:

$$\rho = \frac{\text{MASS}}{\text{AREA}} = \frac{W}{gab} = \frac{.243}{(386)(6)(4)} = 2.623 \times 10^{-5} \text{ Lb SEC}^2/\text{IN}^3$$

The aluminum strips bonded to the board for heat conduction will aid in board stiffness and increase the fundamental resonant frequency. The **bending stiffness values along each board axis and torsional stiffness of the epoxy board and aluminum strip combination is determined as follows:**

With six aluminum strips on the board, the following calculations are based on 1/6 of the board height. The aluminum strips are 0.25 inches wide by 0.050 inches thick.

Item 1 in the following table refers to the epoxy fiberglass board and Item 2 is the aluminum strip.

$$d = \frac{\text{BOARD WIDTH}}{\text{NO. ROWS}} = \frac{4}{6} = .66$$

ITEM	AREA	EX10^6	Z	AEX10^6	AEZX10^6	I_o X 10^{-3}
1	.66X.062 .0409	2.0	.062/2 .031	.0818	.0025	$\frac{.66(.062)^3}{12}$ = .0131
2	.25X.050 .0125	10.5	.062 + $\frac{1}{2}$ .050 .087	.1312	.0114	$\frac{.25(.05)^3}{12}$ = .00260
				.2130	.0139	

ITEM	EI_O X 10^3	C	C^2	AE_c2
1	.0262	.0652 - .031 = .0342	1170 X 10^{-6}	95.71
2	$\frac{.0273}{.0435}$	.087 - .0652 .0218	475 X 10^{-6}	$\frac{62.32}{158.03}$

The centroid of the section is:

$$\overline{Z} = \frac{\sum AEZ}{\sum AE} = \frac{.0139 \times 10^{-6}}{.2130 \times 10^{-6}} = .0652$$

Bending stiffness of the section is:

$$\sum EI = EI_O + AE_C2 = 43.5 + 158.03$$

$$\sum EI = 201.53 \text{ lb } IN^2$$

The bending stiffness of the circuit board along the X axis, with the aluminum strip, is:

$$D_X = \frac{EI}{d} = \frac{201.53}{.66} = \underline{305.35 \text{ lb. in}}$$

AD-A061 349 VOUGHT CORP DALLAS TEX F/G 9/5
STANDARD AVIONIC MODULE STUDY.(U)
MAR 78 D B MCBRAYER, G R COURTNEY, A R TOMME N00123-77-C-0094
UNCLASSIFIED NL

2 OF 2
AD
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2-79
DDC

The bending stiffness along the Y axis will be approximately the same as the epoxy board:

$$D_y = \frac{Eh^3}{12(1-u^2)} = \frac{(2 \times 10^6)(.062)^3}{12\ (1-.12^2)}$$

$$D_y = \underline{40.25}\ \text{lb. in.}$$

Torsional Stiffness

$$Dxy = GeJe + \frac{GrJr}{2d}$$

Where:

$Ge = 0.90 \times 10^6\ \text{lb/in}^2$ - Shear Modulus, Epoxy Fiberglass

$Je = 1/3\ h^3$ - Unit Torsional Stiffness, Epoxy Fiberglass

$Je = 1/3(.062)^3 = 79.3 \times 10^{-6}\ \text{in}^3$

$Gr = 3.5 \times 10^6\ \text{lb/in}^2$ - Shear Modulus, Aluminum Strip

$Jr = 1/3\ Lt^3$ - Torsional Stiffness - Aluminum Strip

$Jr = 1/3(.05)(.25)^3 = 257.81 \times 10^{-6}\ \text{in.}^4$

$d = .66$ in

$$Dxy = (.90 \times 10^6)(79.3 \times 10^{-6}) + \frac{(3.5 \times 10^6)(257.81 \times 10^{-6})}{2(.66)}$$

$$Dxy = 754.96\ \text{lb. in.}$$

Modifying the equation for the fundamental resonant frequency of a circuit board with fixed bottom (Connector) and supported sides (Birtcher Clips) to include stiffness factors due to aluminum strips:[19]

$$f_n = \frac{\pi}{2} \left[\frac{1}{\rho} \left(\frac{Dx}{a^4} + \frac{0.608Dxy}{(a^2)(b^2)} + \frac{0.126Dy}{b^4} \right) \right]^{\frac{1}{2}}$$

$$f_n = 1.57 \left[\frac{1}{2.623 \times 10^{-5}} \left(\frac{305.35}{6^4} + \frac{0.608(754.96)}{(6^2)(4^2)} + \frac{0.126(40.25)}{4^4} \right) \right]$$

$$f_n = 1.57 \left[.381 \times 10^5 \, (.236 + .797 + .198) \right]^{\frac{1}{2}}$$

$$f_n = 1.57 \left[.381 \times 10^5 \, (1.231) \right]^{\frac{1}{2}}$$

$$f_n = 340 \text{ Hz}$$

The maximum allowable circuit board deflection (δ) is equal to 0.003 X the shortest board dimension (4 in.)

$\delta = .003(4) = .012$ in. (Single Amplitude Deflection)

The transmissibility Q is equal to the square root of the fundamental resonant frequency

$$Q = \sqrt{f_n} = \sqrt{340} = 18.44$$

The output G level is calculated from the following:

$$G_{out} = 3\sqrt{\frac{\pi}{2} P f_n Q}$$

Where P = Random power spectral density level

$$P = .15 \ g^2/Hz$$

$$G_{out} = 3\sqrt{\frac{3.14}{2}(.15)(340)(18.44)}$$

$$G_{out} = 115.27$$

The board single amplitude deflection

$$\delta = \frac{9.8 \ G_{out}}{f_n} = \frac{9.8 \ (115.27)}{340^2}$$

$$\delta = 0.010 \text{ in.}$$

4.1.2 Locking Retainer Analysis

The .010 inch single amplitude deflection is marginally acceptable. In order to reduce the deflection to a more acceptable limit, the fundamental resonant frequency needs to be increased. This can be accomplished by increasing the thickness of the board, adding ribs to the board, or by improving board edge retention. The board edge retention can be improved by replacing the Birtcher clips with locking retainers. This will also improve thermal characteristics of the board assembly.

4.1.2.1 Thirty IC Configuration

The addition of locking retainers to the board will reduce the effective "a" dimension of the board by the width of the two retainers. The "a" dimension is now 5.55 inches.

CIRCUIT BOARD WEIGHT CALCULATIONS

$$(5.55 \times 4 \times .062)\ .066 = .091 \text{ lb.} = 1.453 \text{ oz.}$$

IC WEIGHT - Same: 1.214 oz.

ALUMINUM STRIPS: $6 \times 5.55 = 33.3$ in.

$$(33.3 \times .25 \times .05)\ 0.1 = 0.042 \text{ lb.} = 0.666 \text{ oz.}$$

HANDLE - Same: 0.183 oz.

CONFORMAL COATING - Same: 0.112 oz.

TOTAL VIBRATING WEIGHT

$$1.453 + 1.214 + .666 + .183 + .112 = 3.628 \text{ oz.} = 0.227 \text{ lb.}$$

$$\rho = \frac{W}{gab} = \frac{0.227}{(386)(5.55)(4)}$$

$$\rho = 2.649 \times 10^{-5} \text{ lb sec}^2/\text{in.}^3$$

Stiffness factors will be the same as previously calculated

$D_x = 305.35$ lb.in.

$D_y = 40.25$ lb.in.

$D_{xy} = 754.96$ lb.in.

Modifying the equation for the fundamental resonant frequency of a circuit board with fixed bottom edge (connector) and fixed edges (locking retainer) to include stiffness factors due to aluminum strips:[19]

$$f_n = \frac{\pi}{3}\left[\frac{1}{\rho}\left(\frac{.75D_y}{b^4} + \frac{2D_{xy}}{(a^2b^2)} + \frac{12D_x}{a^4}\right)\right]^{\frac{1}{2}}$$

$$f_n = 1.05\left[.378 \times 10^5 \left(.118 + 3.064 + 3.862 \right)\right]^{\frac{1}{2}}$$

$$f_n = 1.05\left[.378 \times 10^5 \left(7.044 \right)\right]^{\frac{1}{2}}$$

$$f_n = 542 \text{ Hz.}$$

MAXIMUM ALLOWABLE SINGLE AMPLITUDE DEFLECTION

$$\delta = .003\ (4) = 0.012 \text{ in.}$$

and the transmissibility is

$$Q = \sqrt{f_n} = \sqrt{542} = 23.28$$

the output G level is

$$G_{out} = 3 \sqrt{\frac{\pi}{2} P f_n Q}$$

$$G_{out} = 3 \sqrt{\frac{3.14}{2} (.15)(542)(23.28)}$$

$$G_{out} = 163.53\ G$$

The expected board single amplitude deflection

$$\delta = \frac{9.8\ G_{out}}{f_n^2}$$

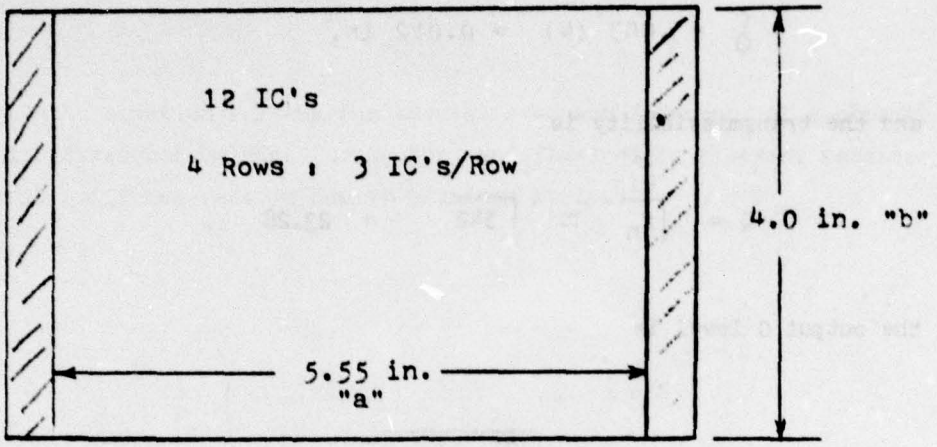
$$\delta = \frac{9.8(163.53)}{542^2} = \frac{1602.6}{293764}$$

$$\delta = 0.005 \text{ in. single amplitude}$$

This deflection is 41% of the allowable deflection and is acceptable.

The deflection levels for the other board configurations considered are also calculated below.

4.1.2.2 Twelve IC Configuration



CIRCUIT BOARD WEIGHT CALCULATIONS

CIRCUIT BOARD - Same - 1.453 oz.

IC WEIGHT = 12(3 grams/DIP) = 36 grams = 1.267 oz.

ALUMINUM STRIPS

$4 \times 5.55 = 22.2$ in.

$22.2 \times .4 \times .05 = .444$ in.$^3 \times .1 = .0444$ lb. $= .710$ oz.

HANDLE: 0.183 oz.

CONFORMAL COATING: 0.112 oz.

TOTAL VIBRATING WEIGHT:

$1.453 + 1.267 + .710 + .183 + .112 = 3.725$ oz. $= .233$ lb.

$$\rho = \frac{W}{gab} = \frac{.233}{(386)(5.55)(4)}$$

$$\rho = 2.72 \times 10^{-5} \text{ lb sec}^2/\text{in.}^3$$

$$d = \frac{\text{Board Width}}{\text{No. Rows}} = \frac{4}{4} = 1.0 \text{ in.}$$

ITEM	AREA	$Ex10^6$	Z	$AEx10^6$	$AEZx10^6$	$I_o x10^{-3}$
1	1x.062 .062	2.0	.062/2 .031	.124	.0038	$\frac{1(.062)^3}{12} = .0199$
2	.4x.05 .020	10.5	.062+½.05 .087	.210 .334	.0183 .0221	$\frac{.4(.05)^3}{12} = .00417$

ITEM	$EI_o \times 10^3$	C	C^2	AEC^2
1	.0398	.0662-.031 .0352	$1239x10^{-6}$	153.64
2	.0438 .0836	.087-.0662 .0208	$433x10^{-6}$	90.93 244.57

The centroid of the section is:

$$\bar{Z} = \frac{\sum AEZ}{\sum AE} = \frac{.0221 \times 10^6}{.334 \times 10^6} = .0662$$

Bending stiffness of the section is

$$\sum EI = EI_o + AEC^2 = 83.6 + 244.57$$

$$\sum EI = 328.17 \text{ lb in.}^2$$

The bending stiffness of the circuit board along the X axis, with the aluminum strip, is

$$Dx = \frac{EI}{d} = \frac{328.17}{1} = 328.17 \text{ lb in.}$$

$Dy = 40.25$ lb in. (prior calculation)

Torsional stiffness

$$Dxy = GeJe + \frac{G_r J_r}{2d}$$

The only change from prior calculations is for J_r

$$J_r = 1/3\ Lt^3 = 1/3\ (.050)(.4)^3$$

$$J_r = 1056 \times 10^{-6} \text{ in.}^4$$

$$Dxy = (.90\times10^6)(79.3\times10^{-6}) + \frac{(3.5\times10^6)(1056\times10^{-6})}{2(1)}$$

$$Dxy = 71.37 + 1848$$

$$Dxy = 1919.4 \text{ lb in.}$$

$$f_n = \frac{\pi}{3}\left[\frac{1}{\rho}\left(\frac{0.75Dy}{b^4} + \frac{2Dxy}{a^2b^2} + \frac{12Dx}{a^4}\right)\right]^{\frac{1}{2}}$$

$$f_n = \frac{3.14}{3}\left[\frac{1}{2.72\times10^{-5}}\left(\frac{.75\times40.25}{4^4} + \frac{2(1919.4)}{5.55^2\times4^2} + \frac{12(328.17)}{5.55^4}\right)\right]^{\frac{1}{2}}$$

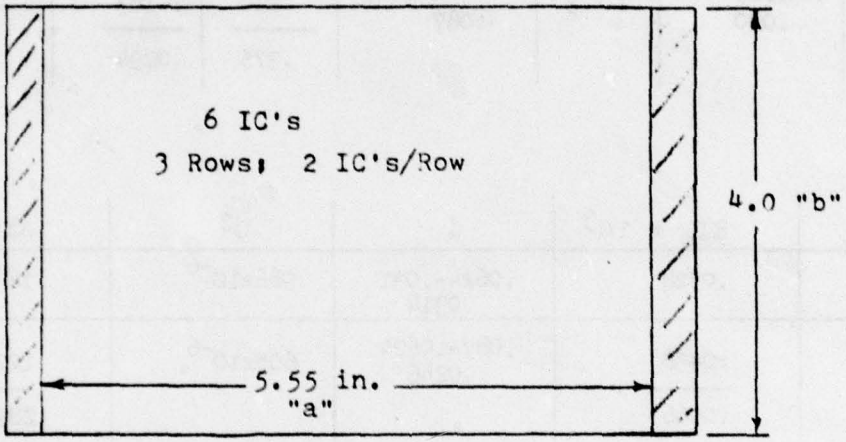
$$f_n = 1.05 \left[.368 \times 10^5 \, (.118 + 7.79 + 4.150) \right]^{\frac{1}{2}}$$

$$f_n = 1.05 \left[.368 \times 10^5 \, (12.058) \right]^{\frac{1}{2}}$$

$$f_n = 699 \text{ Hz}$$

This frequency is higher than that calculated for the thirty IC board and will result in a lower single amplitude deflection.

4.1.2.3 Six IC Configuration



CIRCUIT BOARD WEIGHT CALCULATIONS

CIRCUIT BOARD - Same - 1.453 oz.

IC WEIGHT - 6(6.7) = 40.2 grams = 1.415 oz.

ALUMINUM STRIPS

3 x 5.55 = 16.65 in.

16.65 x .4 x .05 = .333 $in.^3$ x .1 = .0333 lb = .533 oz.

HANDLE - Same - .183 oz.

CONFORMAL COATING - .112 oz.

TOTAL VIBRATING WEIGHT

1.453 + 1.415 + .533 + .183 + .112 = 3.696 oz. = .231 lb.

$$\rho = \frac{W}{gab} = \frac{.231}{(386)(5.55)(4)}$$

$$\rho = 2.69 \times 10^{-5} \text{ lb sec}^2/\text{in}^3$$

$$d = \frac{\text{Board Width}}{\text{No. Rows}} = \frac{4}{3} = 1.333 \text{ in.}$$

ITEM	AREA	$E \times 10^6$	Z	$AE \times 10^6$	$AEZ \times 10^6$	$I_o \times 10^{-3}$
1	1.33x.062 .0825	2.0	.062/2 .031	.165	.0051	$\frac{1.33(.062)^3}{12} = .0264$
2	.4x.05 .020	10.5	.062+½.05 .087	.210 .375	.0183 .0234	$\frac{.4(.05)^3}{12} = .00417$

ITEM	$EI_o \times 10^3$	C	C^2	AEC^2
1	.0528	.0624-.031 .0314	986×10^{-6}	162.7
2	.0438 .0966	.087-.0624 .0246	605×10^{-6}	127.1 289.8

The centroid of the section is at

$$\bar{Z} = \frac{\sum AEZ}{\sum AE} = \frac{.0234 \times 10^{-6}}{.375 \times 10^{-6}} = .0624 \text{ in.}$$

Bending stiffness of the section is

$$\sum EI = EI_o + AEC^2 = 96.6 + 289.8$$

$$\sum EI = 386.4 \text{ lb in.}^2$$

The bending stiffness of the circuit board along the X axis, with the aluminum strip, is

$$Dx = \frac{EI}{d} = \frac{386.4}{1.33} = 290.53 \text{ lb in.}$$

Dy = 40.25 lb in. (prior calculation)

Dxy = 1919.4 lb in. (prior calculation)

$$f_n = \frac{\pi}{3}\left[\frac{1}{\rho}\left(\frac{0.75Dy}{b^4} + \frac{2Dxy}{a^2b^2} + \frac{12Dx}{a^4}\right)\right]^{\frac{1}{2}}$$

$$f_n = \frac{3.14}{3}\left[\frac{1}{2.69\times10^{-5}}\left(\frac{.75\times 40.25}{4^4} + \frac{2\times 1919.4}{5.55^2 4^2} + \frac{12\times 290.53}{5.55^4}\right)\right]^{\frac{1}{2}}$$

$$f_n = 1.05\left[.372\times 10^5\,(.118 + 7.789 + 3.674)\right]^{\frac{1}{2}}$$

$$f_n = 1.05\left[.372\times 10^5\,(11.58)\right]^{\frac{1}{2}}$$

f_n = 689 Hz - Which is acceptable

4.2 Spacing

The allowable spacing between modules in the system is determined primarily by the height of the components. The height for various components[3] is shown in Figure 4.0-2. These values are for the height of the component above the module or board surface only and do not include the thickness of the board or the extension of the leads on the other side of the board. These dimensions must be taken into consideration when defining the module spacing. Typical overall height dimensions for a DIP mounted on an .06 inch board are shown in Figure 4.0-3 with DIP case dimensions from MIL-M-38510A for a 24 pin package. The total top to bottom dimension for this package is 0.425 inches and indicates an 0.5 inch spacing is necessary. If, during the assembly process, the leads could be removed at the back surface of the board eliminating the 0.14 lead extension, the total height would be 0.285 and the module could possibly be used on 0.3 inch centers. It should be noted that this violates existing standards for soldering of leads and also the remaining 0.015 inches between the top of the DIP and the bottom of the board complicate both the mechanical design of the module/rack and significantly affects the ability to cool the devices by convection. Also, these dimensions do not account for any conformal coating layer on the DIP or any shielding which might be required for EMI/EMP protection. Because of these considerations and in an attempt to define a standard module program consistent with all present IC package technologies, it is recommended that the standard spacing be set at 0.4 inches. For special cases such as power supplies, etc., which require large discrete components multiple slots of 0.4 inches can be assigned.

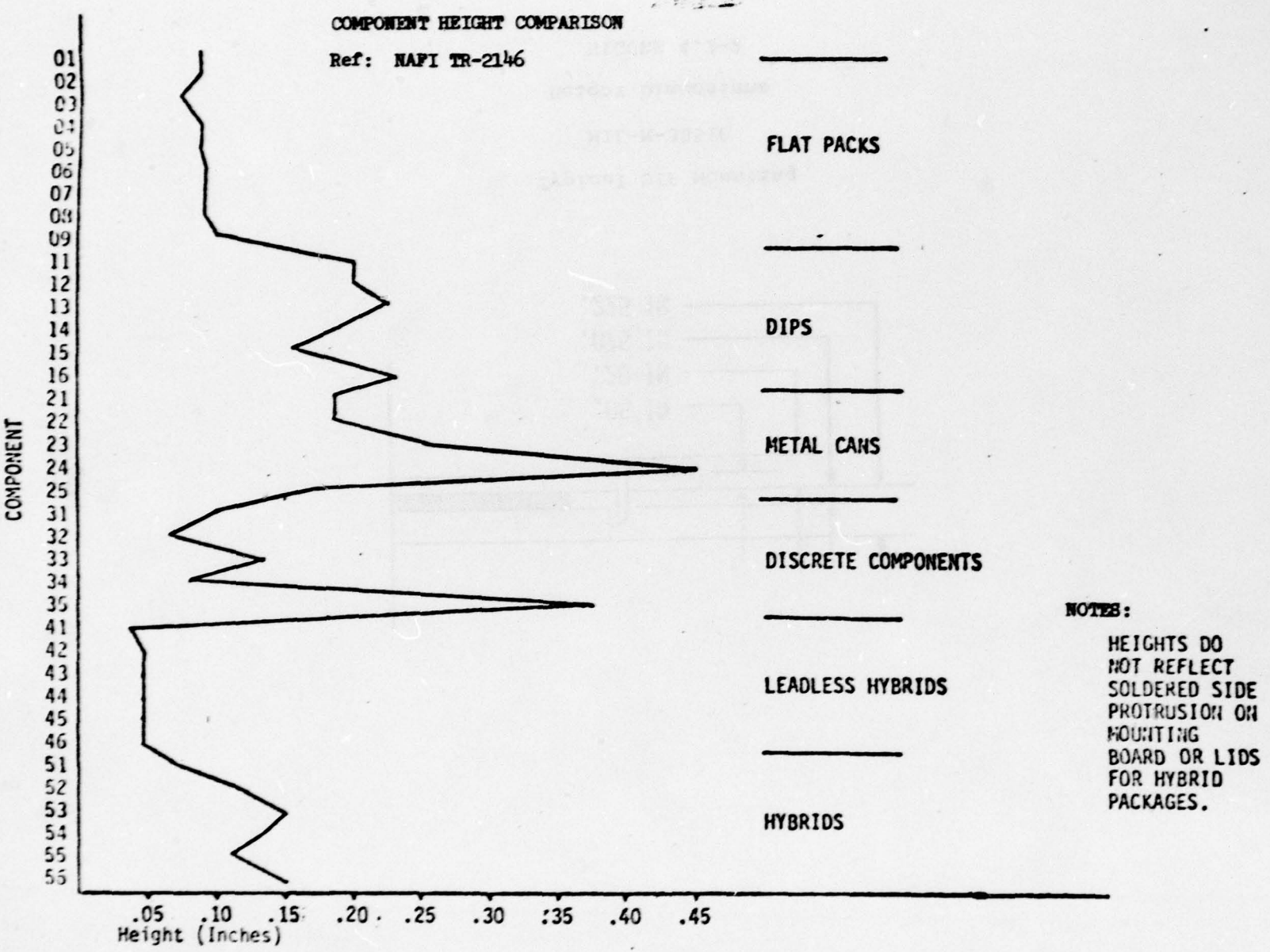
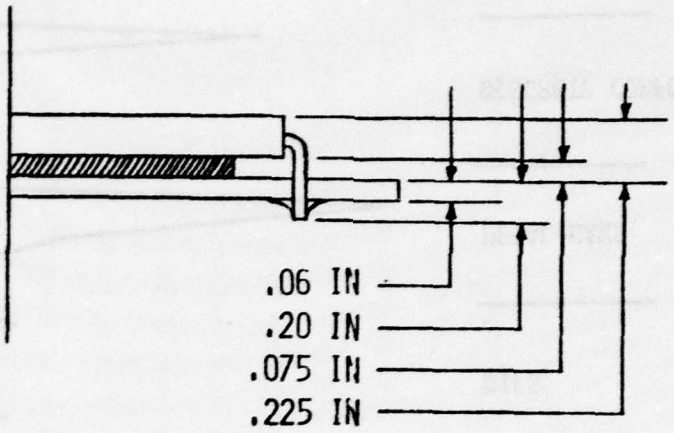

COMPONENT HEIGHT COMPARISON
Ref: NAFI TR-2146
COMPONENT
01
02
03
04
05
06
07
08
09
11
12
13
14
15
16
21
22
23
24
25
31
32
33
34
35
41
42
43
44
45
46
51
52
53
54
55
56
FLAT PACKS
DIPS
METAL CANS
DISCRETE COMPONENTS
LEADLESS HYBRIDS
HYBRIDS
NOTES:
HEIGHTS DO NOT REFLECT SOLDERED SIDE PROTRUSION ON MOUNTING BOARD OR LIDS FOR HYBRID PACKAGES.
.05
.10
.15
.20
.25
.30
.35
.40
.45
Height (Inches)

FIGURE 4.2-1



Typical DIP Mounting

MIL-M-38510

Height Dimensions

FIGURE 4.2-2

5.0 MODULE COMPARISON WITH DATA BASE MODULES

The Data Base and Reference reports contain the mechanical and functional descriptions of several proposed and/or existing modules. The recommended module described herein is compared with these modules in the following paragraphs.

5.1 Physical Comparison

The physical size of 35 modules are described in the Data Base and Reference reports not including those which exhibit only minor modifications to another module. These 35 modules are tabulated in Table 5.1-1 with the report describing the module referenced. The distribution of these modules as a function of width and height are shown in Figure 5.1-1. The recommended module is the same size as the Module 7 recommended by Honeywell[2]. Of the remaining 34 modules, 27 are larger in either height or width and only 7 are smaller or equal in both height and width. These modules are:

1 NADC Configuration A1 for 3/8 ATR

2 NADC Configuration B1 for 1/2 ATR

10 Honeywell - Improved SEM 2A

12 Raytheon Type I

18 NAFI TR 2173 SEM 1A

20 IBM SEM 1A

29 Hughes High Power 1/2 ATR

Of the 35 modules, 13 have total board areas less than or equal to that of the recommended configuration. It is also interesting to note that the recommended configuration has an aspect ratio (width/height) similar to 5 of the other modules at 0.66.

The active area provided by each of the 35 modules is shown in Figure 5.1-2. The average area for this group of modules is 22.9 square inches compared to the 17.6 square inches recommended. This difference occurs because several of the modules in the Data Base and Reference reports are sized for compatibility with the 3/4 ATR or larger equipment housings.

This comparison of physical size indicates that the recommended module is near the mean value of other modules considered in length, width, aspect ratio and area and is consistent with the previous studies.

Table 5.1-1

Summary of Module Sizes

Evaluated, Currently Used or Recommended

Module Size	Source of Module	Ref. Report	(IN) Width	(IN) Height	(IN^2) Area	PINS	Comments
1	NADC Configuration A1	1	2.687	2.75		40	Compatible with 3/8 ATR
2	NADC Configuration B1	1	4.0	2.75		92	Compatible with 1/2 ATR
3	NADC Configuration D1	1	6.625	2.75		142	Compatible with 3/4 ATR
4	NADC Configuration D2	1	6.625	4.0		142	Compatible with 1/2 ATR
5	NADC Configuration D4	1	6.625	6.5		142	Compatible with 3/4 ATR
6	NADC Configuration F4	1	9.25	6.5		192	Compatible with 1 ATR
7	Honeywell	2	6.0	4.0		150	
8	NAFI TR 2146 (DIP/75% Eff.)	3	--	--	14.6	102	
9	NAFI TR 2146 (FP/75% Eff.)	3	--	--	11.9	102	
10	Honeywell ISEM 2A	4	5.34	1.30		100	
11	Raytheon IBMS	5	7.26	5.6		120	
12	Raytheon TYPE I	5	4.5	4.0		66	
13	Raytheon TYPE II	5	7.25	6.0		120	
14	NAFI TR 2173 CONCEPT #1	6	7.06	4.19	14.8	100	
15	NAFI TR 2173 CONCEPT #6	6	7.62	4.78	18.0	165	
16	NAFI TR 2173 Improved SEM (2A)	6	6.64	2.88	7.0	100	
17	NAFI TR 2173 HAC MODULE	6	6.0	7.35	29.8	100	
18	NAFI TR 2173 SEM 1A	6	3.0	2.88	2.2	40	
19	GE (AIDS STUDY)	7	6.78	4.55	--	50	Similar to 1/2 ATR (D2), Module Size 4 above
20	IBM SEM 1A Modified	9	3.596	2.325		40	
21	IBM SEM 2A Modified	9	7.056	2.325		100	
22	NELC QED Modified	9	6.756	5.325		80	
23	IBM ML-1 240	9	7.625	4.438		240	
24	IBM ML-1 Modified	9	7.625	4.438		160	
25	Westinghouse 1/2 ATR	10	3.6	6.2		140	
26	Westinghouse 3/4 ATR	10	6.2	6.2		140	
27	Westinghouse 1 ATR	10	9.0	6.2		140	
28	Westinghouse 1½ ATR	10	14.2	6.2			
29	Hughes High Power 1/2 ATR	14	5.12	3.4			
30	Hughes High Power 3/4 ATR	14	5.12	6.0			
31	Hughes High Power 1 ATR	14	6.91	6.17			
32	Hughes Low Power 1/2 ATR	14	6.50	3.40			
33	Hughes Low Power 3/4 ATR	14	6.50	6.0			
34	Hughes Low Power 1 ATR	14	8.70	6.17			
35	Hughes Advanced Technology Module	14	9.0	5.2			

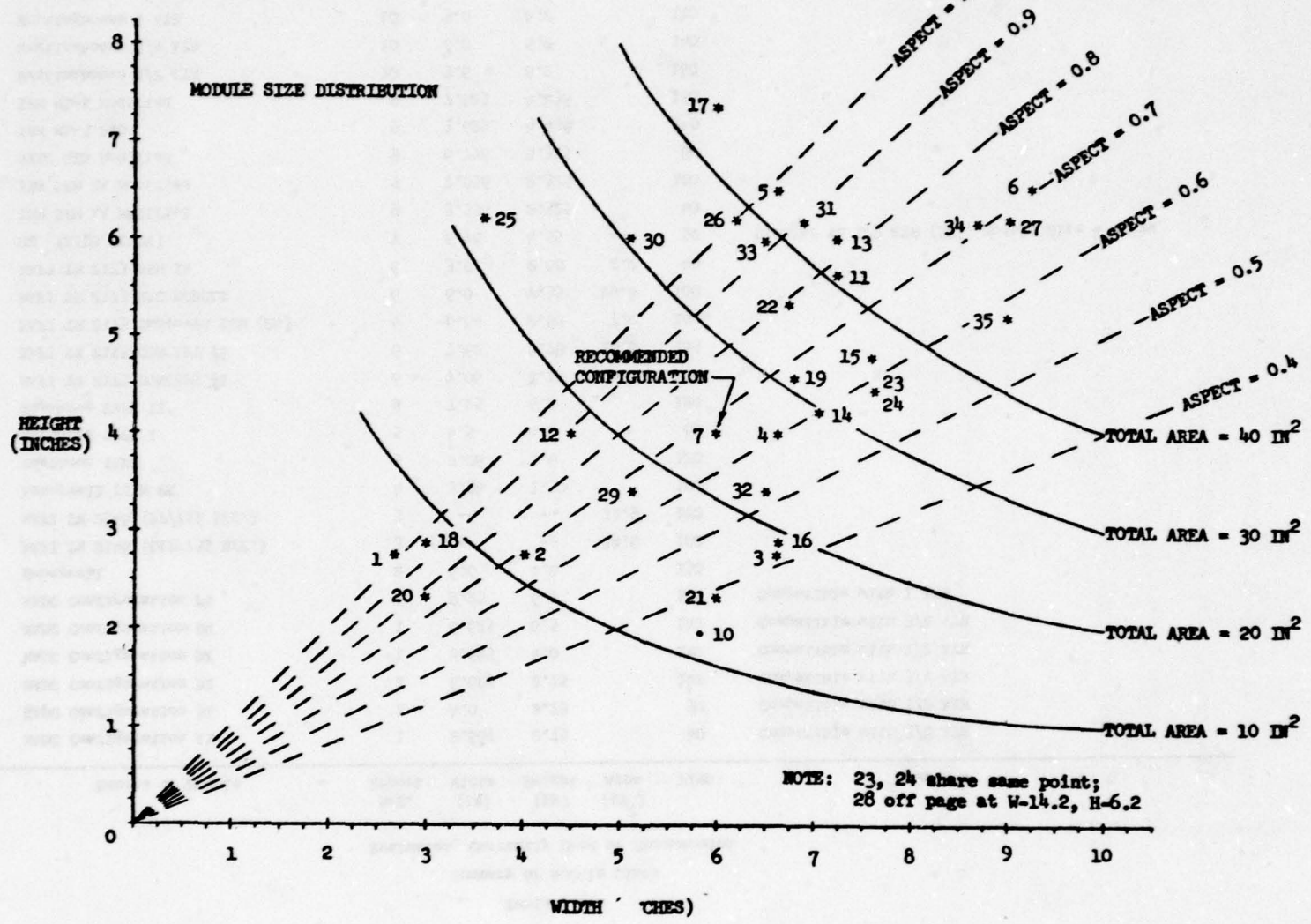

MODULE SIZE DISTRIBUTION
HEIGHT (INCHES)
WIDTH (INCHES)
ASPECT = 1.0
ASPECT = 0.9
ASPECT = 0.8
ASPECT = 0.7
ASPECT = 0.6
ASPECT = 0.5
ASPECT = 0.4
TOTAL AREA = 40 IN²
TOTAL AREA = 30 IN²
TOTAL AREA = 20 IN²
TOTAL AREA = 10 IN²
RECOMMENDED CONFIGURATION
NOTE: 23, 24 share same point;
28 off page at W-14.2, H-6.2

FIGURE 5.1-1

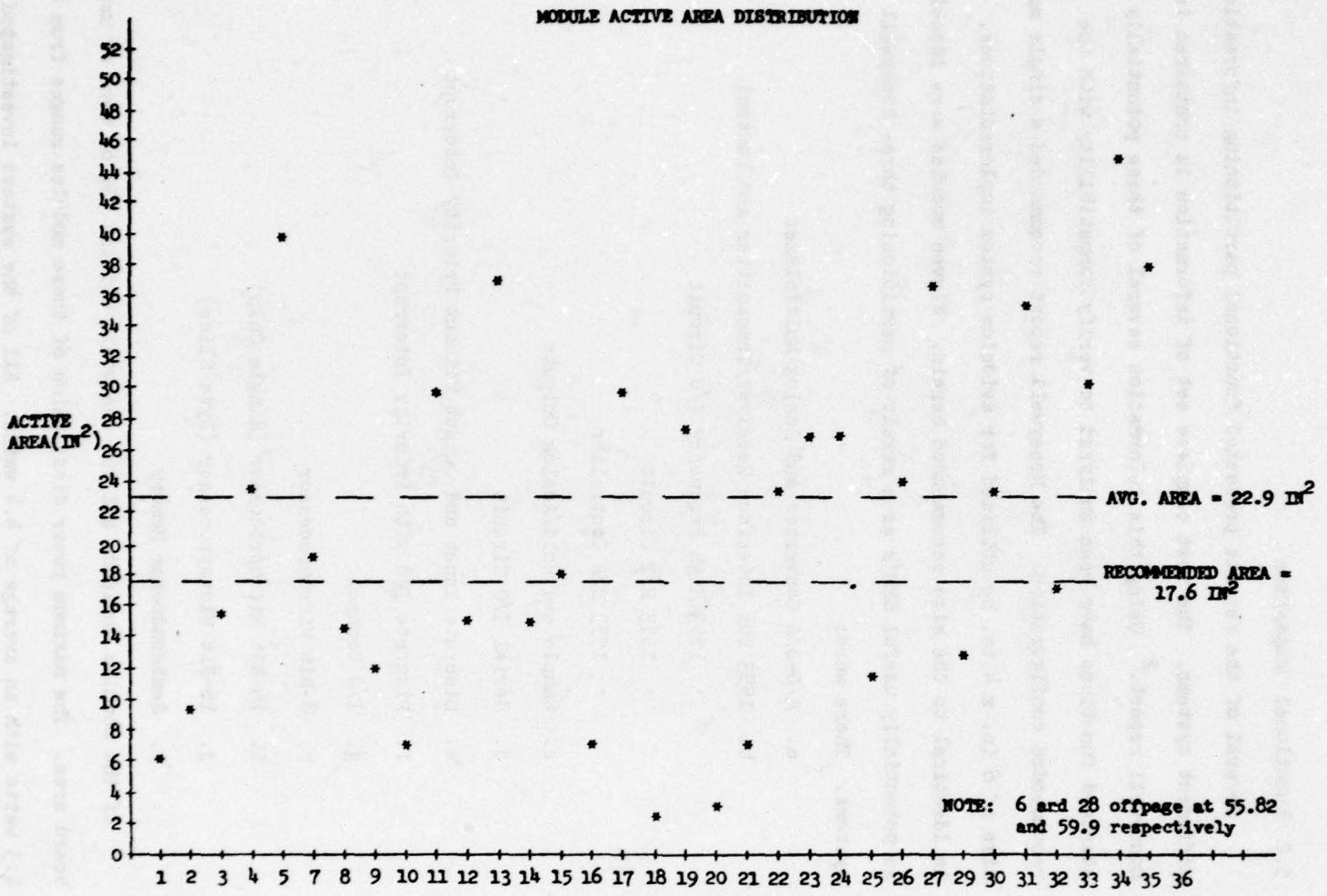

MODULE ACTIVE AREA DISTRIBUTION
ACTIVE AREA(IN²)
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
52
AVG. AREA = 22.9 IN²
RECOMMENDED AREA = 17.6 IN²
NOTE: 6 ard 28 offpage at 55.82 and 59.9 respectively
1 2 3 4 5 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 29 30 31 32 33 34 35 36
MODULE NO.

FIGURE 5.1-2

5.2 Functional Comparison

Several of the reports presented functional partitioning information on different systems. The most complete set of information is contained in the Honeywell report.[2] Using this information several of these potentially standard functions have been analyzed to verify compatibility with the recommended configuration. The Honeywell report recommended a single module size of 6 in. x 4 in. be utilized for avionics system implementations. This is identical to the size recommended herein. Eleven modules were identified as potentially useful SEM's as a result of partitioning three Honeywell systems. There were:

a. A/D-D/A Converter and Analog Multiplexer

b. 1553 Bus Interface Receiver/Transmitter and Control

- 1553 High Frequency I/O Circuit
- 1553 R/T Circuit
- 1553 DMA Controller

c. Sample and Hold/Analog Outputs

d. Serial I/O Circuit

e. Discrete Input and Output Without Priority Interrupt

f. Discrete I/O with Priority Interrupt

g. I/O Control

h. 8-Bit Microprocessor

i. 16-Bit Microprocessor (Single Chip)

j. 16-Bit Microprocessor (Byte Slice)

k. Semiconductor Memory

Of the modules defined, all but one would utilize 75% or more of usable board area. The maximum power dissipation of these modules ranges from 8.3 to 1.3 watts with an average of 4.4 watts. All of the systems investigated must either transmit data to other systems or receive data from other systems or

both. As a result, the 1553 Interface Function (Module b) should be the most widely used of all the modules defined. This module was divided by Honeywell into two sections: A single board design using three custom LSIC's and a three board design using currently available components.

The Honeywell estimate of components required for the first seven of these proposed modules is listed in Tables 5.2-1 thru 5.2-10. Preliminary physical layouts, Figures 5.2-1 thru 5.2-9, for six of these modules were completed as part of this study. Usable board area on the proposed 6 in. by 4 in. module precluded layout of the Honeywell Module e., "Discrete I/O, Without Priority Interrupt" primarily because of the large number of discrete components required for this function. It is assumed that these components could be packaged into a hybrid or thick film module to minimize the component mounting area.

A tabulation of the potentially standard, or common, functions which are identified in the Data Base and Reference reports and compatible with the recommended configuration is presented in Table 5.2-11. The functions discussed in the previous paragraph are included in this tabulation. The anticipated power dissipation and required number of pins for electrical interface is included for those functions for which the information is available. The source report for the function is referenced in each case of the 44 functions identified. From the partitioning information the average board area utilization is 79%. This utilization factor is slightly higher than the 70% value which is considered an acceptable minimum. For these 44 functions, the average connector pin requirement is 62 and the average power dissipation is 5.7 watts.

This analysis indicates that the recommended module configuration is compatible with the standard functions which have been identified in previous studies and provides good utilization of board area, thus minimizing system volume.

GE[7] described several low voltage and high voltage power supplies which are not included in the tabulation since they are not compatible with the module spacings anticipated for the SAM program. These power supplies are compatible, in general, with the height and width of the recommended configuration but will require special installation provisions.

The Telephonics report[8] describes a functional partitioning of the General Purpose Multiplex System (GPMS) which resulted in the establishment of 3 standard modules; Post Module, On-Line Processor (ONL) Module, and Off-Line Processor (OFL) Module. These modules provide the system designer with sufficient flexibility to configure terminals for any mode required. The detail design of the circuits for these modules is not described. However, the description indicates that the design is anticipated to be compatible with the Standard Electronic Module (SEM) configuration. This discussion, in conjunction with work being conducted by other contractors on LSI circuits in accordance with MIL-STD-1553A and GPMS, indicates that the multiplex terminal circuit can easily be packaged into the SAM configuration.

TABLE 5.2-1

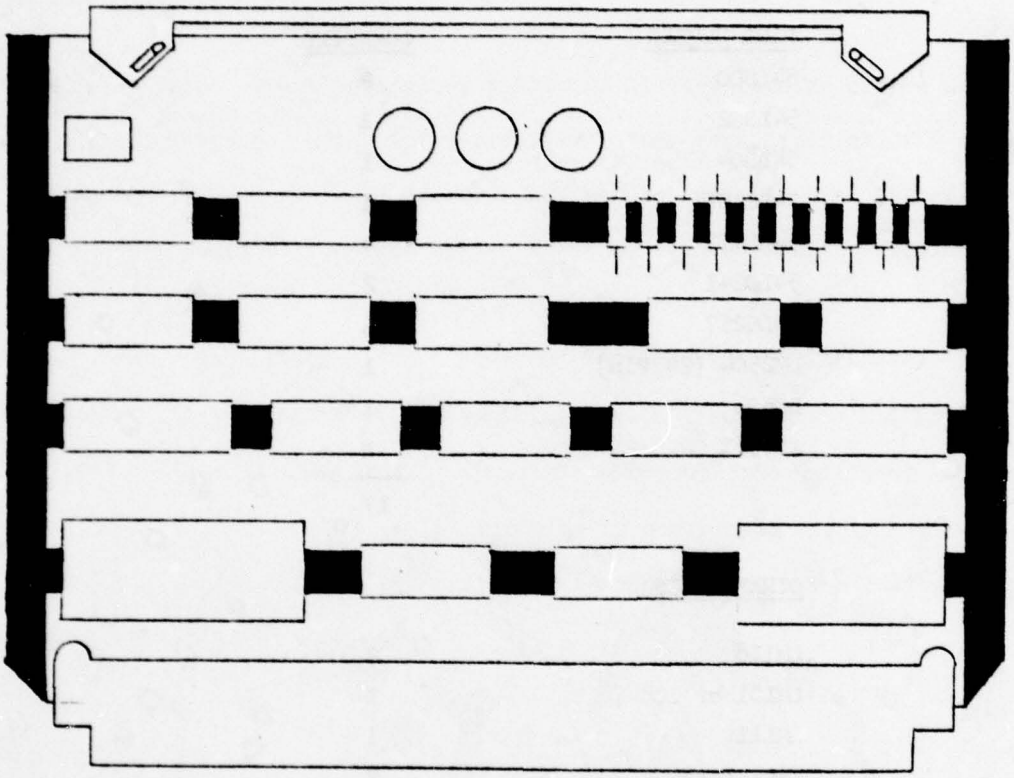
A/D-D/A, Analog MUX

I/O Pins = 73 Power Dissipation = 3 watts

PART NUMBER	QUANTITY
54LS00	2
54LS02	1
54LS04	1
54LS109	1
54LS173	4
54LS241	2
54LS257	3
DM2504 (24 Pin)	1
DG506	1
AD7521	1
	17

OTHER PARTS

LM118	2
LM101 or 108	1
LM111	1
Resistors	7
Diodes (1N645 or 1N4001)	2
Zener Diode (1N821)	1
TOTAL:	31



A/D - D/A, ANALOG MUX

FIGURE 5.2-1

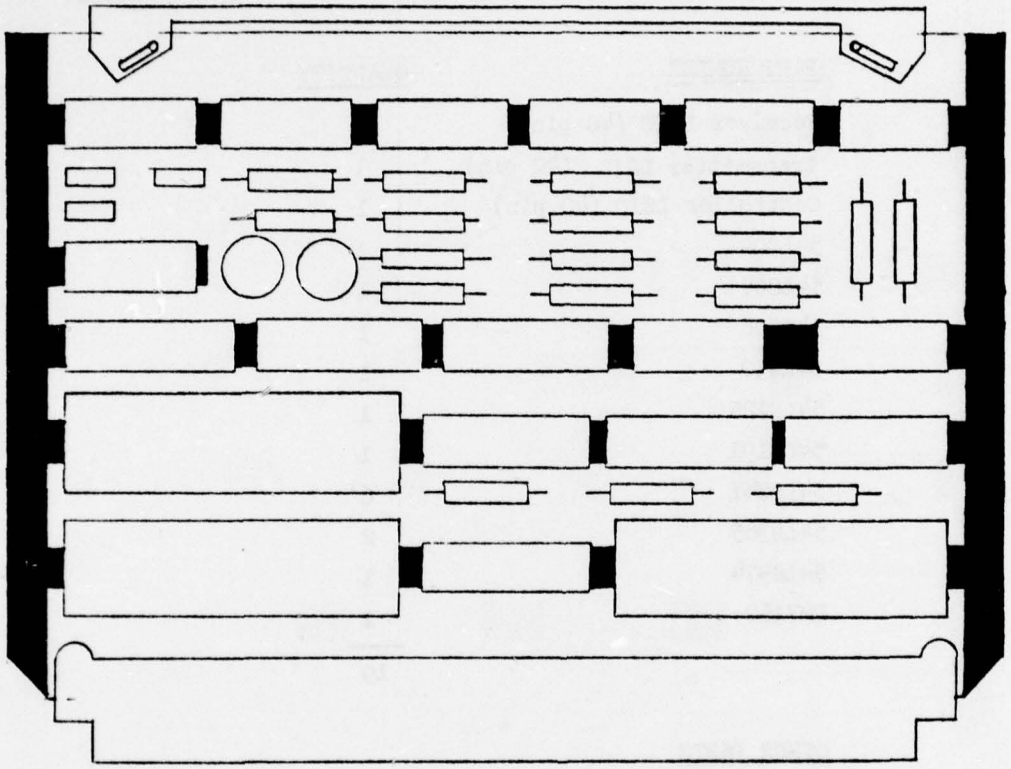
TABLE 5.2-2

SINGLE 1553 R/T and CONTROLLER

I/O Pins = 65 Power Dissipation = 5 watts

PART NUMBER	QUANTITY
Receiver LSIC (40 pin)	1
Transmitter LSIC (40 pin)	1
Controller LSIC (40 pin)	1
54LS04	1
54LS05	1
54LS08	1
54LS30	1
54LS125	1
54LS191	1
54LS241	6
54LS365	2
54LS374	1
DM7160	1
	19

OTHER PARTS	
LM111	2
Capacitor	3
Resistors	15
NPN Transistors	2
Diodes	2
TOTAL:	43



SINGLE 1553 R/T AND CONTROLLER

FIGURE 5.2-2

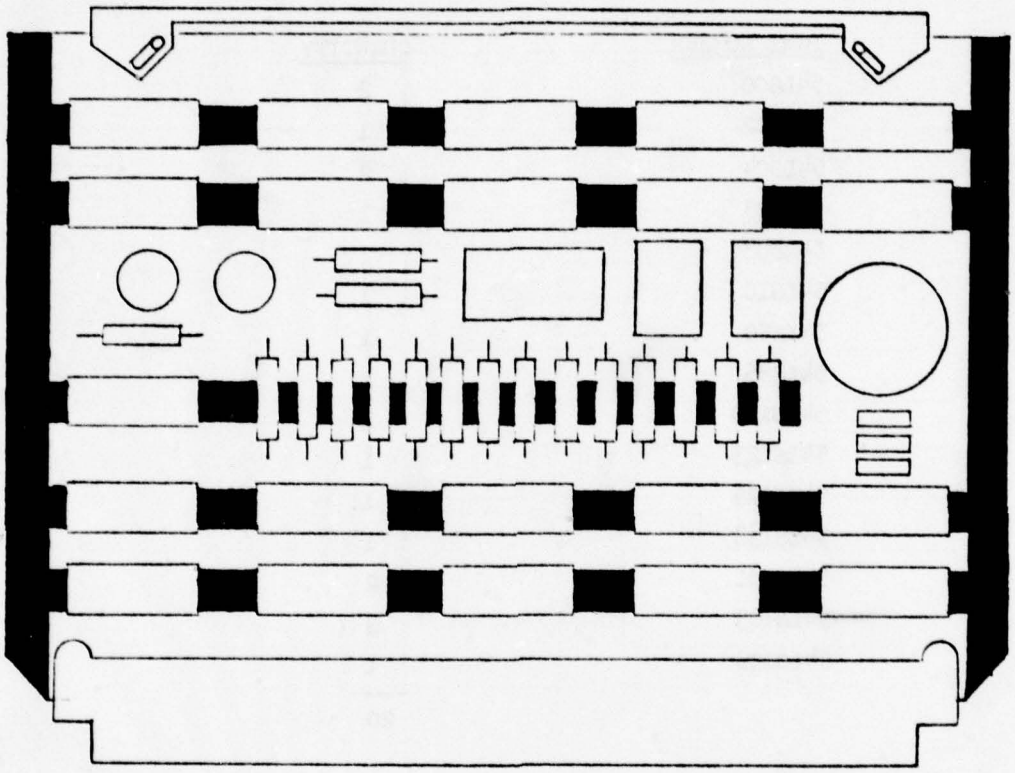
TABLE 5.2-3

1553 H-F I/O CIRCUIT

I/O Pins = 19 Power Dissipation = 2.7 watts

PART NUMBER	QUANTITY
54LS00	2
54LS02	1
54LS04	2
54LS05	1
54LS08	1
54LS10	1
54LS50	1
54LS86	1
54LS109	1
54LS123	1
54LS125	1
54LS138	1
54LS151	2
54LS163	3
54LS195	1
	20

OTHER PARTS	
Oscillator	1
Crystal	1
Transformer	1
Capacitor	3
LM111	2
NPN Transistor	2
Diodes	2
Resistor	15
TOTAL:	47



1553 H-F I/O CKT

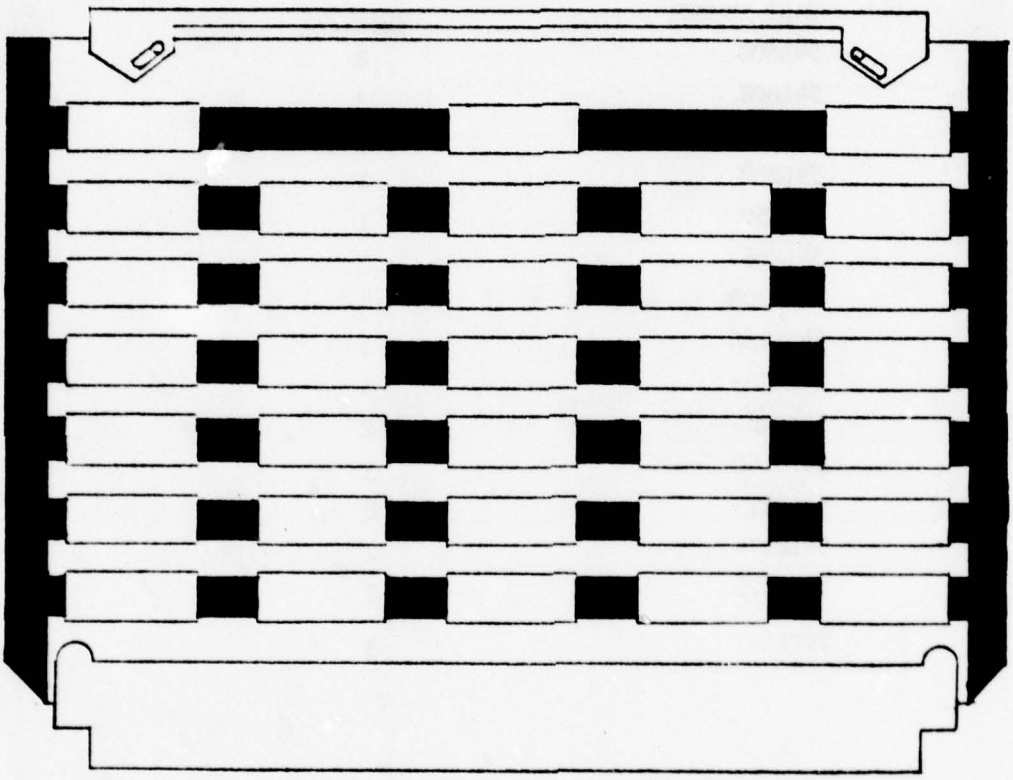
FIGURE 5.2-3

TABLE 5.2-4

1553 R/T CIRCUIT

I/O Pins: 50 Power Dissipation: 3.1 watts

PART NUMBER	QUANTITY
54LS00	2
54LS02	3
54LS04	3
54LS08	1
54LS50	1
54LS86	1
54LS109	4
54LS162	1
54LS163	1
54LS164	2
54LS166	3
54LS173	8
54LS174	1
54LS175	2
TOTAL:	33



1553 R/T CKT

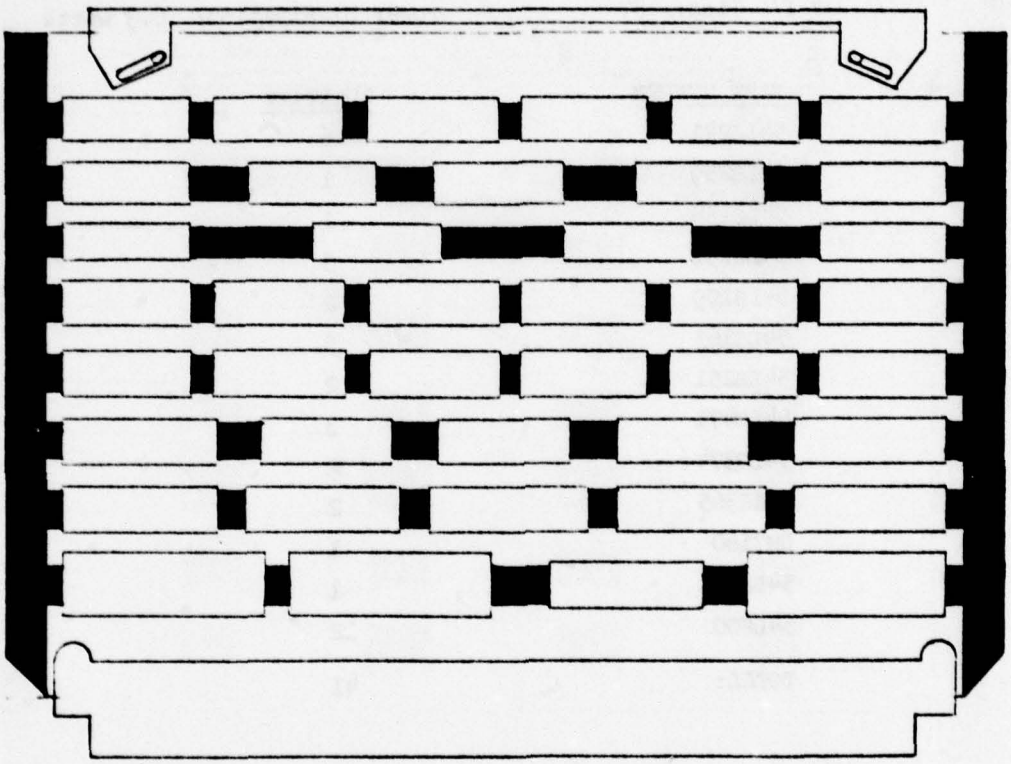
FIGURE 5.2-4

TABLE 5.2-5

1553 DMA CONTROLLER

I/O Pins: 87 Power Dissipation: 6.3 watts

PART NUMBER	QUANTITY
54LS241	6
54LS259	1
54LS138	1
54LS191	3
54LS109	2
54LS163	5
54LS251	2
54LS471	3
54LS374	2
54LS365	2
DM7160	1
54LS174	1
54LS00	12
TOTAL:	41



1553 DMA CONTROLLER

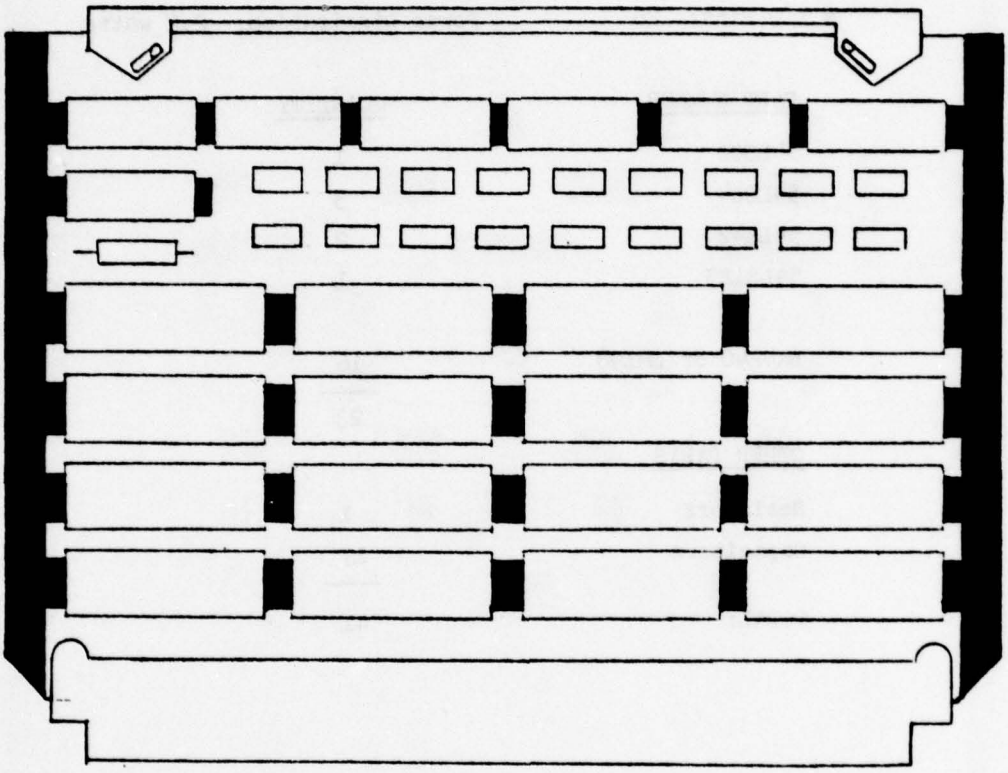
FIGURE 5.2-5

TABLE 5.2-6

SAMPLE HOLD ANALOG OUTPUTS

I/O Pins: 26 Power Dissipation: 2.2 watts

PART NUMBER	QUANTITY
54LS00	1
54LS04	3
54LS42	2
54LS123	1
HA4240 or LM198	16
	23
OTHER PARTS	
Resistors	1
Capacitors	17
TOTAL:	41



SAMPLE HOLD ANALOG OUTPUTS

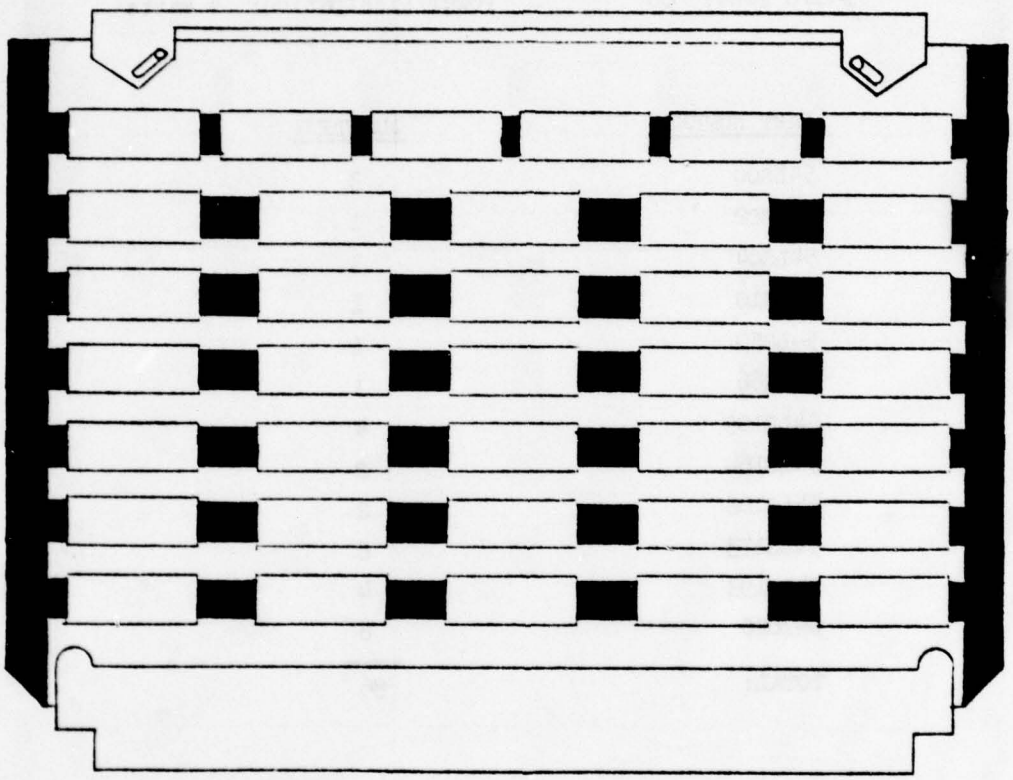
FIGURE 5.2-6

TABLE 5.2-7

SERIAL I/O CIRCUIT

I/O Pins: 60 Power Dissipation: 4 watts

PART NUMBER	QUANTITY
54LS00	3
54LS02	1
54LS04	3
54LS10	1
54LS50	1
54LS86	1
54LS109	4
54LS164	2
54LS166	2
54LS173	8
54LS193	4
DM7820	6
TOTAL:	36



SERIAL I/O CIRCUIT

FIGURE 5.2-7

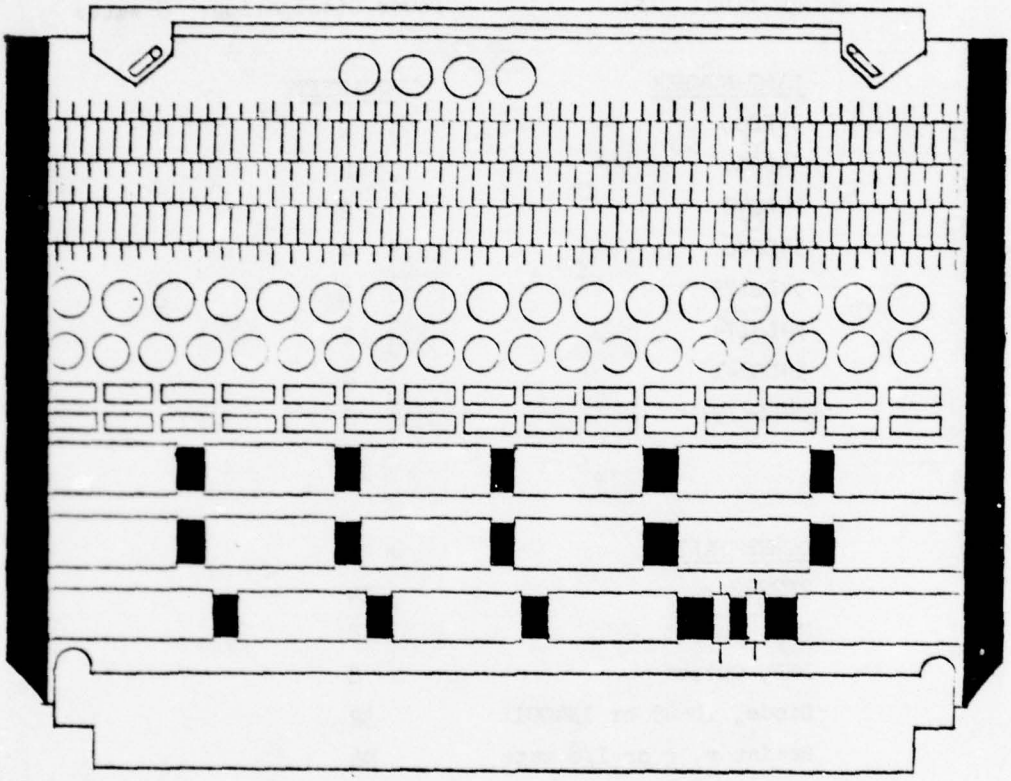
TABLE 5.2-8

DISCRETE I/O WITH INTERRUPT OUTPUT

I/O Pins: 53 Power Dissipation: 8 watts

PART NUMBER	QUANTITY
54LS00	2
54LS04	2
54LS42	2
54LS86	4
54LS173	1
54LS174	2
54LS241	2
54LS279	2
	17

OTHER PARTS	
2N2222	24
NPN, Output	8
PNP, Output	8
Diode, 1N645 or 1N4001	32
Resistor, $\frac{1}{4}$ or 1/8 watt	96
Resistor, $\frac{1}{2}$ watt	16
TOTAL:	201



DISCRETE I/O WITH INTERRUPT OUTPUT

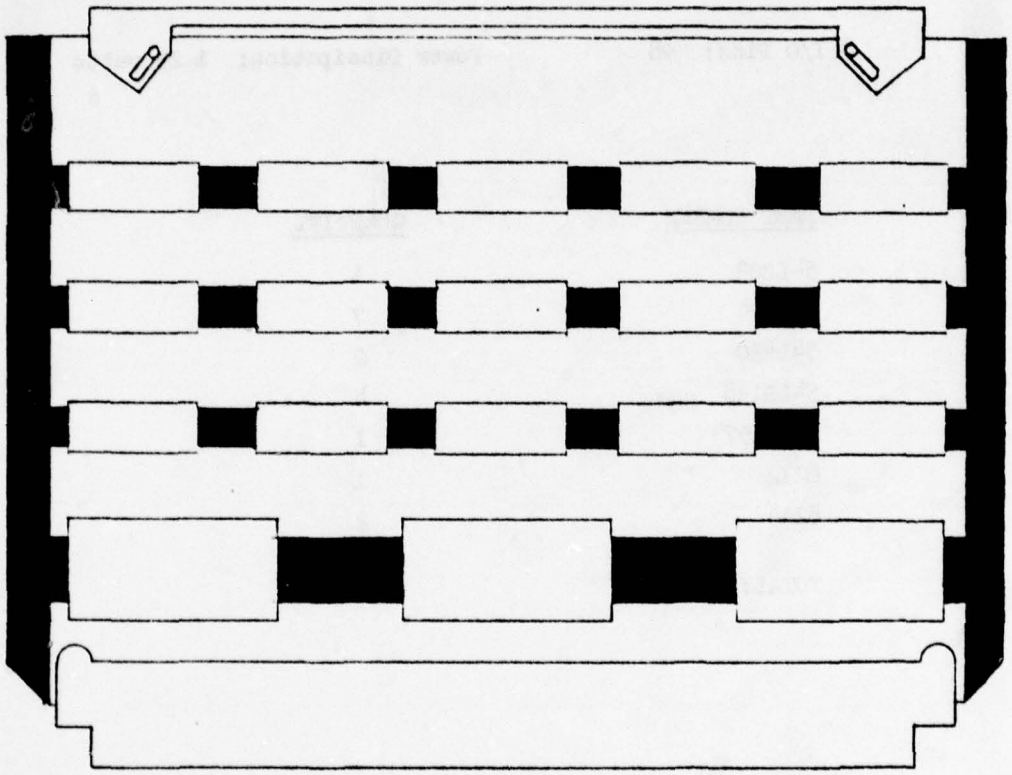
FIGURE 5.2-8

TABLE 5.2-9

I/O CONTROL

I/O Pins: 98 Power Dissipation: 1.25 watts

PART NUMBER	QUANTITY
54LS02	1
54LS04	7
54LS30	2
54LS138	4
54LS157	1
8212	1
8214	2
TOTAL:	18



I/O CONTROL

FIGURE 5.2-9

TABLE 5.2-10

DISCRETE I/O's, WITHOUT PRIORITY INTERRUPT

I/O Pins: 61 Power Dissipation: 8.3 watts

PART NUMBER	QUANTITY
54LS00	1
54LS04	4
54LS10	2
54LS42	4
54LS241	2
54LS279	4
	17

OTHER PARTS

2N2222	32
NPN, Output	16
PNP, Output	16
Diode, 1N645 or 1N4001	48
Resistors, 1/8 or 1/4 watt	154
Resistors, 1/2 watt	32
TOTAL:	315

Table 5.2-11

Potential Standard or Common Functions

Function Ident.	Function Description	Reference Report	Estimated % Board Utilization	Estimated Pin Count	Estimated Power (Watts)	Comments
1	A/D - D/A Analog Multiplexer	2	75	73	3.0	Board utilization estimates are Honeywell estimates for similar size module
2	1553A High Frequency I/O	2	75	19	2.7	Board utilization estimates are Honeywell estimates for similar size module
3	1553A Receiver/Transmitter	2	80	50	3.1	Board utilization estimates are Honeywell estimates for similar size module
4	1553A DMA Controller	2	90	87	6.3	Board utilization estimates are Honeywell estimates for similar size module
5	Sample & Hold Analog Circuit	2	75	26	2.2	Board utilization estimates are Honeywell estimates for similar size module
6	Serial I/O	2	90	60	4.0	Board utilization estimates are Honeywell estimates for similar size module
7	Discrete I/O without Priority Int.	2	95	61	8.3	Board utilization estimates are Honeywell estimates for similar size module
8	Discrete I/O with Priority Int.	2	90	53	8.0	Board utilization estimates are Honeywell estimates for similar size module
9	I/O Control and Priority Int.	2	40	98	1.3	Board utilization estimates are Honeywell estimates for similar size module
10	8-Bit Microprocessor	2	--	--	--	-
11	16-Bit (Single Chip) Microprocessor	2	--	--	--	
12	16-Bit High Performance Microprocessor (Byte slice)	2	--	--	--	
13	Semiconductor Memory Module	2	--	--	--	
14	Microprocessor - ALU	5	84			Board utilization based upon estimated component count
15	Microprocessor - Control Unit	5	84			Board utilization based upon estimated component count
16	Microprocessor - Memory - 4K	5	100			Board utilization based upon estimated component count
17	Microprocessor - Peripheral I/P	5	100			Board utilization based upon estimated component count
18	Bit DC Voltage Monitor	5	84			Board utilization based upon estimated component count

Table 5.2-11 - (Continued)

Function Ident.	Function Description	Reference Report	Estimated % Board Utilization	Estimated Pin Count	Estimated Power (Watts)	Comments
19	Multiplexed Analog Transmission by Serial Digital Bus	5	100	--	--	Board utilization based upon estimated component count
20	Logarithmic Crystal Video Receiver	5	80	--	--	Board utilization estimated for LSI
21	Video Pulse Train Sorter	5	100	--	--	Board utilization estimated for thick film
22	Pulse Receiver, Video Detector and Measurement Encoder	5	100	--	--	Board utilization based upon estimated component count
23	General Purpose Range Technique Modulation Generator	5	100	--	--	Board utilization based upon estimated component count
24	General Purpose Angle Technique Modulation Generator	5	100	--	--	Board utilization estimated for thick film
25	General Use 6 - 4 Bit Binary Counter, 3 - 4 Bit Up/Down Counters	6	77	90	5.1	
26	Memory Address and Digital Scan Converter X-Y Control and X Address Generator	6	70	38	6.6	
27	Memory Address and Digital Scan Converter Y Address Generator	6	70	58	7.65	
28	TV Address Generator - Serial In/Parallel Out, Parallel Data In Compare	6	80	77	8.4	
29	TV Address Generator - Control, Mux/Demux and Bus Driver	6	67	73	3.2	
30	DSC Chain Generator - Register, Mux, Full Address and BIT	6	64	63	5.6	
31	DSC Chain Generator - Co-Ordinate Transform	6	100	37	5.1	May require some hybridization
32	Symbol Processor - Shift Register, 9 - 4 Bit Serial to Parallel	6	30	74	1.0	
33	Symbol Processor - Decoder	6	50	67	4.9	
34	Symbol Processor - D/A Video Conversion and Dynamic Shift Register	6	57	48	--	
35	Special Symbol Timing - Parallel - Serial Storage and Compare	6	83	64	7.5	

Table 5.2-11 - (Continued)

Function Ident.	Function Description	Reference Report	Estimated % Board Utilization	Estimated Pin Count	Estimated Power (Watts)	Comments
36	RAM Memory (4K x 24) with both Parallel and Serial Out	6	90	88	9.6	
37	RAM Memory (4K x 24) Control	6	77	72	12.8	
38	Controller RAM - Timing & Control, Address Selector, Refresh Address, Refresh Control	6	93	92	5.9	
39	Controller RAM - Memory & Buffers	6	73	42	9.1	
40	Analog Scaler, Integrator and Analog Multiplex	6	61	62	12.3	
41	Controller ROM - 2K x 8 Bit ROM Memory	6	50	20	5.62	
42	Controller ROM - Memory Data Bus, I/O Buffers, Multiplexers	6	30	69	5.0	
43	Video Processor	7	100	--	--	May require LSI and/or hybridization
44	Deflection Amplifier	7	100	--	--	May require LSI and/or hybridization

6.0 DESIGN CONSIDERATIONS

The actual mechanical design of a standard module must consider the effects of the use environment consisting of vibration, shock, humidity, temperature, altitude, etc. Also, of extreme importance is the EMI/EMP/EMV environment in which the module is to operate. The effects of these considerations on the design and the recommended levels for test are described in the following paragraphs.

6.1 Environmental

The data base reports generally recommend that the Standard Avionics Modules be designed to meet the environmental test requirements of MIL-E-5400R, for Class 2 equipment.

Vibration test requirements vary from report to report but most agree that a random vibration test provides the SAM with the more realistic actual use vibration environment. The random vibration level recommended by a majority of the data base reports is in the range of 0.15 G^2/Hz from 50 to 1,000 Hz, dropping to .001 G^2/Hz at 2000 Hz.

The Hughes Aircraft Company Report[14] "Function and Configuration Analysis Program", provides significant detail on the description and justification of dynamic test requirements for the SAM. The report states that the dynamic test requirements should be sufficiently general is that the module, qualified to these requirements, could be incorporated into avionics equipment which might be installed in any location in any aircraft, fixed or rotary wing. Based upon the numerous factors that influence the dynamic environment of a module, a set of practical requirements for a module must be a gross simplification of the actual environment. The Hughes Report recommends only random vibration to satisfy the dynamic test requirements. The belief is that shock and acoustic test requirements would not yield significant results. The sinusoidal vibration test is discounted for reasons that if the sine vibration levels are reasonably specified, the dynamic effect on the module will be less severe than the recommended random vibration.

All other environmental tests are as specified by MIL-E-5400R. However, MIL-E-5400R is meant to be a "general" military specification, to be used as a guide to design and test. The procuring agency is responsible for specifying deviations to spec requirements to be consistent with the avionics environment exposure.

Conformal Coating is required on the modules to satisfy the humidity and salt spray test requirements of MIL-E-5400F for ceramic parts. These components, in particular, are very sensitive to moisture adsorption and are required by paragraph 3.1.15.1 of MIL-E-5400F to be sealed and moisture proofed. For Army procurements, all wiring assemblies, including multilayer, are required by requirement 17 of MIL-STD-454E to be conformally coated. To satisfy humidity and salt spray requirements without conformal coating each module, the modules would have to be assembled in hermetically sealed units, which is not consistent with the maintainability concepts for military aircraft especially VSTOL. The proposed use of the modules in environmentally controlled cabinets or racks which may be opened to the environment at the "O" level exposes the modules to salt-sea air. The conformal coating of the module with thicknesses less than .003 inches will have no appreciable adverse affect on convection cooling of the module if that cooling method is used.

Listed below are recommended Environmental Qualification Test Requirements for the Standard Avionics Module:

Temperature	MIL-E-5400R - Para. 3.2.24.1 - Class 2
Altitude	MIL-E-5400R - Para. 3.2.24.2 - Class 2
Temperature-Altitude Combined	MIL-E-5400R - Para. 3.2.24.3 - Class 2
Humidity	MIL-E-5400R - Para. 3.2.24.4 - Class 2
Vibration	Random only: 0.15 g^2/Hz 50 - 1000 Hz: 3 Hrs/Axis
Salt Atmosphere	MIL-E-5400R - Para. 3.2.24.9
Explosive Conditions	MIL-E-5400R - Para. 3.2.24.10

The test procedures for the above tests shall be per MIL-T-5422 for the Navy, and MIL-STD-810 for the Air Force and Army.

6.2 EMC Considerations

The standard avionics module concept as part of an overall integrated rack provides for some interesting EMC considerations. With an attitude of "it can be done but a cautious approach is necessary", the following observations are offered:

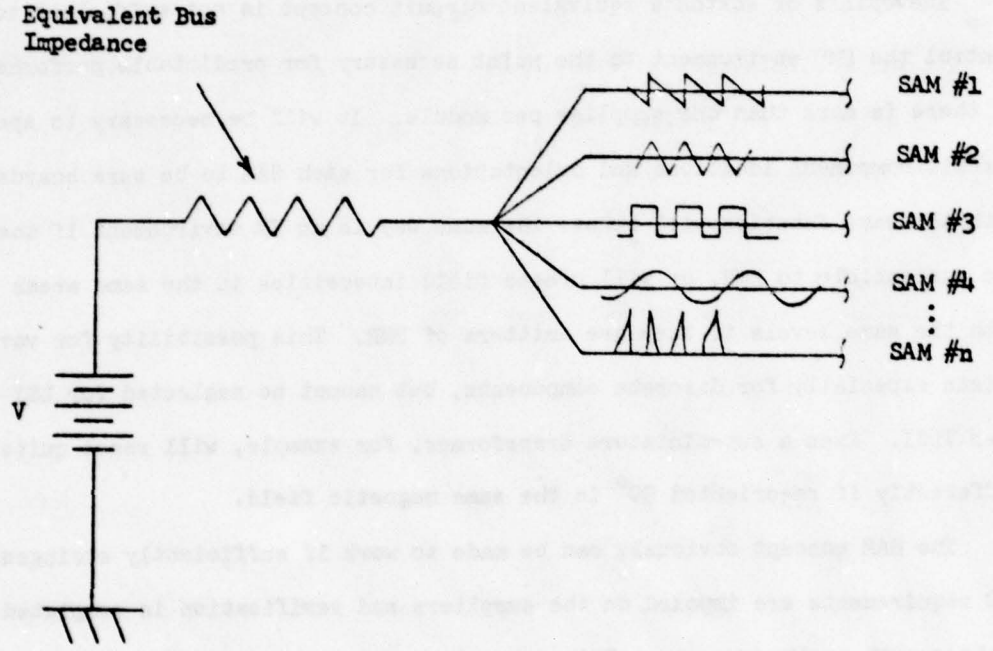
Thevenin's or Norton's equivalent circuit concept is not sufficient to control the EMC environment to the point necessary for predictable performance if there is more than one supplier per module. It will be necessary to specify circuit/component locations and orientations for each SAM to be sure boards with the same function will behave the same way in an EM environment if they are susceptible to EMR, or will create field intensities in the same areas and with the same levels if they are emitters of EMR. This possibility for variance exists especially for discrete components, but cannot be neglected for LSI or even VLSI. Even a sub-miniature transformer, for example, will react quite differently if re-oriented 90° in the same magnetic field.

The SAM concept obviously can be made to work if sufficiently stringent EMC requirements are imposed on the suppliers and verification is completed early enough in the program. This concept, however, is not cost effective. A more viable approach is to use a combination of reasonable specification requirements, computer analyses, and segregated or compartmentalized areas for SAM's of the same EMC classification. An example of how this could potentially be implemented follows:

MIL-STD-461/462 requirements and tests could not be implemented per se. The basic concept of controlling conducted and radiated emanations and susceptibilities is necessary, however, and will have to be achieved. This

FIGURE 6.2-1

TYPICAL WAVEFORMS ON SAM POWER LINES



will involve preparing a new set of specifications along the following guide lines:

- o A government/industry developed power bus emissions limit could be used to define the limit of which a SAM could emit or be subjected. For simplicity sake, this should be a time-domain type specification and this type data could be gained in early breadboard stages inexpensively and therefore incorporated into the analysis phase in a timely manner.
- o It is possible today to use computer techniques to analyze a large number of SAM-type installations connected to a common bus and analytical techniques that will be available in the 1980's will be much more powerful. Figure 6.2-1 illustrates a possible model for this approach. If the power source for the SAM's were a true voltage source, i.e., zero internal impedance, there would be no bus impedance coupling, obviously. Since a finite impedance does exist, however, some coupling will exist between the various modules. Computer codes are available that will predict the amount of coupling that will occur and the amount of decoupling necessary to achieve compatibility.
- o Radiated environments compatibility could be achieved by classifying SAM's according to whether they are interference sources or they are susceptible to interference and segregating the same classes into the same areas of the integrated racks. This technique is presently used in cable routing and connector pin classification to a good degree of success.
- o Present MIL-STD-462 radiated emission and susceptibility test methods could be used with relaxed levels. It is recommended, however, that each SAM be required to meet only one, possibly two, of these methods to obtain early, inexpensive results.

6.2.1 Anticipated V/STOL Environments

Based on the A-7E background, previous RFP's, and recent customer contacts, the following environments are expected to be applicable to V/STOL design.

Electromagnetic Pulse (EMP) - This is a transient phenomenon caused by interaction of nuclear radiation (such as gamma ray) with the air. It is a pulse of very short duration but one of very large amplitudes. It is expected V/STOL requirements will be specified as 50,000 volts per meter peak for an exo-atmospheric nuclear event. This will typically produce skin currents on the order of several thousand amperes on an aircraft of V/STOL size.

Electromagnetic Vulnerability - V/STOL design will require compliance to MIL-HDBK-235 (classified) levels which include carrier deck environments. These levels include both continuous wave (CW) and pulse fields of very high amplitudes.

Lightning - Much work is presently being done in the USA and the United Kingdom in defining amplitudes and waveforms. The exact requirements for the V/STOL time frame is difficult to define at present, therefore, but expected amplitude maximums will be between 200,000 and 400,000 amperes.

Hazards of Electromagnetic Radiation to Ordnance (HERO) - The V/STOL weapon systems will ultimately be tested at the Naval Surface Weapons Center to certify that it is safe for carrying ordnance devices. These tests will cover the frequency range of 0.25 MHz to 10 GHz and varies in amplitude from 1-300 V/m, CW, up to 32 MHz, and 0.01 to 150 milliwatts/cm^2 for frequencies from 225 MHz to 10 GHz.

Static Electricity - An airframe can be subjected to hundreds of thousand volts potential difference with respect to the surrounding air or isolated, ungrounded areas within the airframe. This voltage can be caused by triboelectric conditions, fluids flowing in or over a surface. Effects can range from static annoyances

in communication equipment, damage to wind shield and electrical components, detonation of explosive devices, to personnel shock.

Secure Speech Requirements - Cryptographic communication capabilities will be required for the V/STOL and NSA requirements will be enforced. Very substantial isolation between coded and clear signals will be required, therefore, if such functions are incorporated within the rack assembly.

Nuclear Environments other than EMP -

o Transient Radiated Effects on Electronics (TREE) - Particle radiation levels are generally classified for a particular application, but V/STOL requirements will probably include neutron fluence values of 10^{12} n/cm^2 and prompt gamma dose rates of 10^9 rads/sec.

o System Generated EMP (SGEMP) caused by ionizing radiation interaction with system materials will probably not be defined separately from the EMP and TREE environments but will have to be considered in the overall, combined effects of the system response to a nuclear event.

o Blast and Thermal Effects - These effects are attendant with any nuclear event. Effects on SAM's are expected to be no different than present design techniques, however, except that larger volumes are involved which will respond to vibration and shock loads differently than a smaller unit.

6.2.2 Application Guide Lines

An integration contractor will be necessary to assemble data, perform analyses and verification tests at the integrated rack level, and also to determine rack interface requirements. Aircraft design considering the specified environments must be implemented early in the design stages using the following guidelines:

o Use a single point ground concept for the overall airplane design. This makes sense especially with the extensive use of composites anticipated

in the aircraft. In practice, there may be more than one such ground, but they should be kept to a minimum. The signal ground, or a principal one, should be in the integrated rack area, i.e., close to the principal computer(s).

o Separate and balanced power leads should be used, i.e., do not share a common return, and should be routed as twisted pairs. This minimizes EMP and EMV coupling and will reduce the protection required at the rack level.

o Signal and control leads should be routed as twisted shielded pair, generally speaking, and an overall braid will be required on the most sensitive wires.

Integrated rack design should consider the following:

o Interface circuits should utilize fiber optic design to the maximum extent. This will greatly reduce the possibility of EMP, EMV and all forms of EMC from entering the rack assembly.

o Integrated rack enclosure will have to be of a metal design to provide the shielding necessary for EMP and EMV environments. Ionizing radiation effects on the enclosure material will have to be considered in light of SGEMP generation. This phenomenon will have to be included in the overall analysis to cover synergistic and combined effects.

o Power line and other interface wires that cannot be designed to use fiber optics or optical couplers will need adequate filtering, other protection devices such as zener or TransZorb* clamps, or a combination of techniques to prevent EMP from entering the rack. A certain amount of terminal protection will be required at the SAM level.

o The integration contractor should collect and provide up-to-date data base information to SAM suppliers so they can choose components that will meet applicable ionizing radiation environments.

* TransZorb is a registered trademark of General Semiconductor Industries, Inc.

7.0 CONCLUSIONS

This study has reviewed the data and information accumulated during several previous studies performed by other companies and government ogranizations. The various factors which affect the size of the module have been analyzed and conclusions reached on each factor. These intermediate conclusions are:

Functional Commonality - The packaging concept should provide for a maximum of 30 IC's per module to achieve any savings in total ownership cost.

Connector - The number of pins required to electrically interface the module into the system can be estimated by the relationship;

$$PINS = 3.8\ G^{r},$$

where $0.58 > r > 0.52$

The connector type should be the NAFI blade and fork with 0.1 inch pin spacing.

Integrated Circuit Packaging Technology - Present technology is 14-16 pin IC with an average of approximately 18 gates per IC. The 1985 technology is projected to be a 40 pin IC with an average of approximately 100 gates per IC. The dual-in-line package will be more widely used than flatpacks. The chip carrier package can provide a higher gate density package.

Weight and Volume Constraints - The module active area should be greater than 10 square inches (more than 20 dual-in-line IC's) to minimize effect of overhead volume.

Thermal Considerations - Thermal conduction requirements can be satisfied within size limitations set by IC count using DIP packaging.

Built-In-Test - The inclusion of BIT increases the complexity and size of a system by 15 to 25%.

Reliability - The module should contain 27 or less 14-16 pin IC's using TTL logic with maximum junction temperatures of 105° C. With junction temperatures of 85° C, the maximum number of 14-16 pin IC's can be increased to 30.

By comparing these intermediate conclusions with preliminary partitioning information, a module capability of 30 14 to 16 pin dual-in-line integrated circuits with a 100 pin connector was established. The mechanical development of this module resulted in a 4 inch (height) by 6 inch (width) module which can be installed on 0.4 inch centers. This module is designed to withstand the anticipated environmental requirements and is capable of dissipating approximately 15 watts of power by thermal conduction to the housing. The resulting module compares favorably, both mechanically and functionally, to other modules described in the Data Base and Reference reports.

8.0 RECOMMENDATIONS

In the process of performing this study several areas of concern in the establishment, implementation and maintenance of a successful standard avionic module program have been identified. These items should be resolved prior to the initiation of the design of any module or the specification preparation for systems which are to use the SAM concept. These issues are:

a. EMI/EMP - A thorough analysis of the system requirements for protection against the effects of EMI/EMP/EMV is required. An attenuation budget should be established for each phenomena for the aircraft skin, for the avionic enclosure and for the individual module. In addition, typical environments experienced on a module-to-module basis for electromagnetic radiation, susceptibility, conduction, etc., should be established for the board spacings to be used in the SAM program. Each board must be controlled, by specification, similarly to the requirements of MIL-STD-461/462 presently used for individual equipments. This includes consideration of power line ripple, power transients, etc. It is recommended that this area of concern be resolved by a program to (1) analytically determine the design requirements for the overall system, the rack enclosure and individual modules, (2) design, construct and test a typical SAM subsystem mounted in a rack enclosure and (3) prepare EMI Specifications. The subsystem utilized for this demonstration should include those circuit types which generally create problems from an EMI standpoint, such as, power supplies, interface data receivers and transmitters, etc.

b. Maintenance Philosophy - The maintenance philosophy for all systems using the SAM concept must be established prior to the initiation of design of any standard module or system utilizing the standard module. Decisions must be made on the built-in-test concept which is to be used. It must be remembered that a module designed under one maintenance/BIT concept may not be capable of use under another maintenance/BIT concept. It is recommended that a program be initiated to prepare a detail specification for the maintenance and BIT requirements for the overall avionic system, individual systems and individual modules. This document should define what portions of BIT are to be accomplished in hardware, what portion is to be accomplished in software, and if fault isolation techniques such as visual/audible indicators, are to be used.

c. Environmental - The effects of exposure to the anticipated thermal, vibration, humidity, and salt-sea atmosphere on the SAM design concept should be evaluated. It is recommended that a test program be initiated to perform environmental tests, on an engineering basis, on an avionic rack containing a typical subsystem. This rack should simulate to the best extent the design concepts to be used in a typical SAM installation. This program could be part of and an extension of the EMI/EMP/EMV testing described above. The test program should be of such length and intensity to thoroughly analyze the long term, as well as short term, effects on the equipment.

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APPENDIX A
THERMAL CALCULATIONS

The following thermal calculations are based upon cooling a single six inch by four inch epoxy fiberglass board by conduction only. This is accomplished by the lamination of aluminum strips on the board to transfer the heat from the board components to the side wall through a locking retainer. Thermal calculations have been completed for three different board configurations: thirty, sixteen pin IC's; twelve, twenty-four pin IC's; and six, forty pin IC's. The connector used in all three configurations is the NAFI blade and fork with 100 pins on 0.1 inch centers. The overall connector width of 5.44 inches is one of the determining factors in the final configuration 6 inch width of the module. A minimum of 0.25 inches is required along each edge of the module to install the locking retainers. Table A-1 provides both the design requirements and the total power dissipation capability for each module configuration. The maximum gate junction temperature for all cases is 105° C with a temperature of 71° C at the surface of the housing.

Thirty IC Module

The following calculations are based upon installing thirty, sixteen pin, dual-in-line packages (DIPS) as shown in Figure A-1. The aluminum conducting strips are 0.25 inches in width by 0.05 inches thick. The DIPS are installed on the board with an 0.001 inch film of thermal joint compound between the component case and the aluminum conducting strip to decrease the gap resistance. The calculations are based on one-half of one row of DIPS and assume that the middle DIP divides its power dissipation equally with one-half of the total going to each side wall.

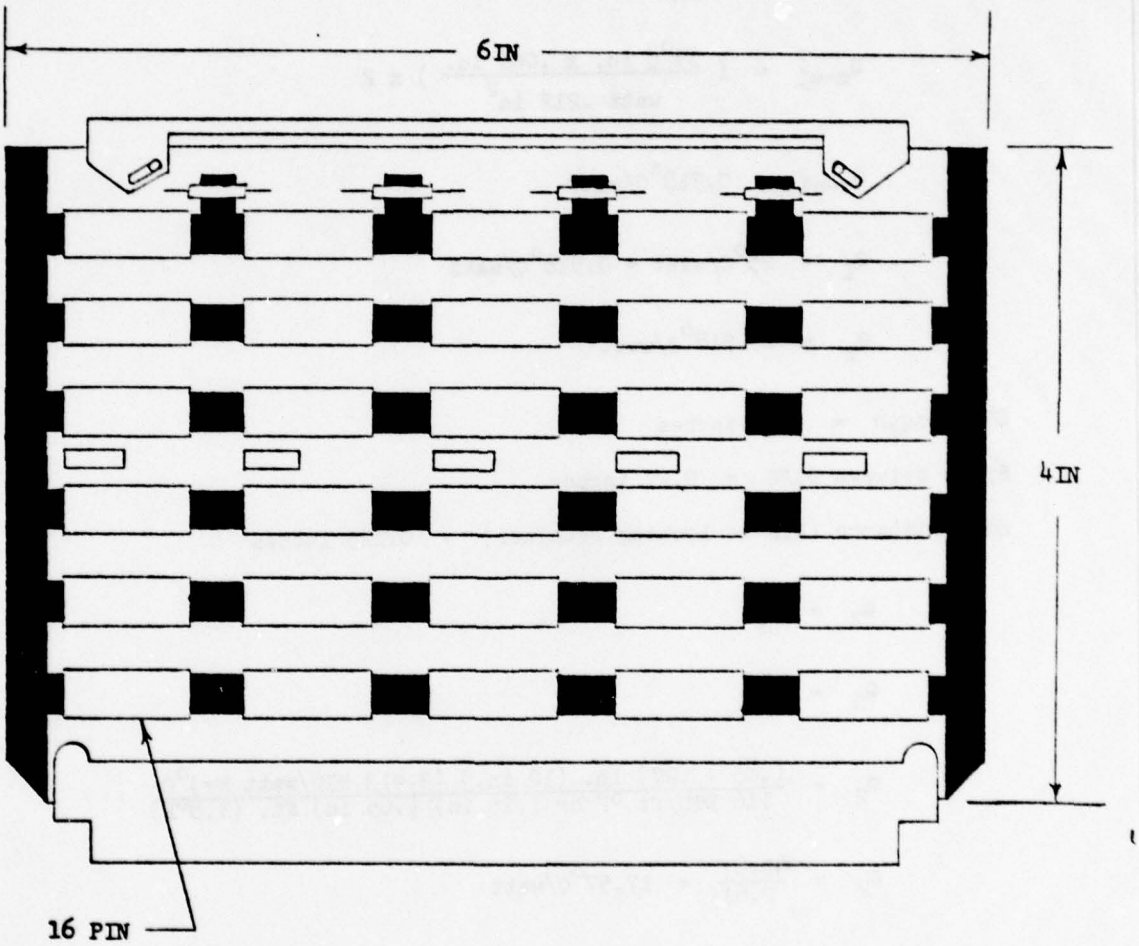
From Table A-1, the total power dissipation required for this configuration is 10.68 watts.

$$\frac{10.68 \text{ watts}}{30 \text{ DIPS}} = 0.356 \text{ watts/DIP}$$

IC's	I/O Count	Gates/IC	Total Gates	MW/Gate	Total Power Dissipation Required (watts)	Power Dissipation Capability (watts)
30	16	17.8	534	20	10.68	10.96
12	24	40	480	20	9.60	12.6
6	40	100	600	20	12.00	13.35

Power Dissipation
Requirements & Capability

TABLE A-1



THIRTY DUAL IN-LINE PACKAGE INSTALLATION
POWER DISSIPATION - 10.68 WATTS

FIGURE A-1

each SAM be required to meet only one, possibly two, of these methods to obtain early, inexpensive results.

The thermal model used in the analysis of this configuration is shown in Figure A-2. The calculations follow:

$$\theta_{c\text{-}al} = \left(\frac{\rho t}{A}\right) \times 2^{*}$$

$$\theta_{c\text{-}al} = \left(\frac{55^{\circ}C \text{ in.} \times .001 \text{ in.}}{\text{watt } .212 \text{ in}^2}\right) \times 2$$

$$\theta_{c\text{-}al} = 0.518^{\circ}C/\text{watt}$$

$$\theta_1 = 25^{\circ}C/\text{watt} + 0.518^{\circ}C/\text{watt}$$

$$\theta_1 = 25.518^{\circ}C/\text{watt}$$

DIP length = 0.85 inches

Space between DIPS = 0.27 inches

Edge Distance (DIP to locking retainer) = 0.125 inches

$$\theta_2 = \theta_4$$

$$\theta_2 = \frac{L}{KA}$$

$$\theta_2 = \frac{(.85 + .27) \text{ in. } (12 \text{ in.}) \ (3.413 \text{ BTU/watt hr})^{\circ}C}{116 \text{ BTU/ft } {}^{\circ}F \text{ hr } (.25 \text{ in}) \ (.05 \text{ in}) \text{ ft. } (1.8^{\circ}F)}$$

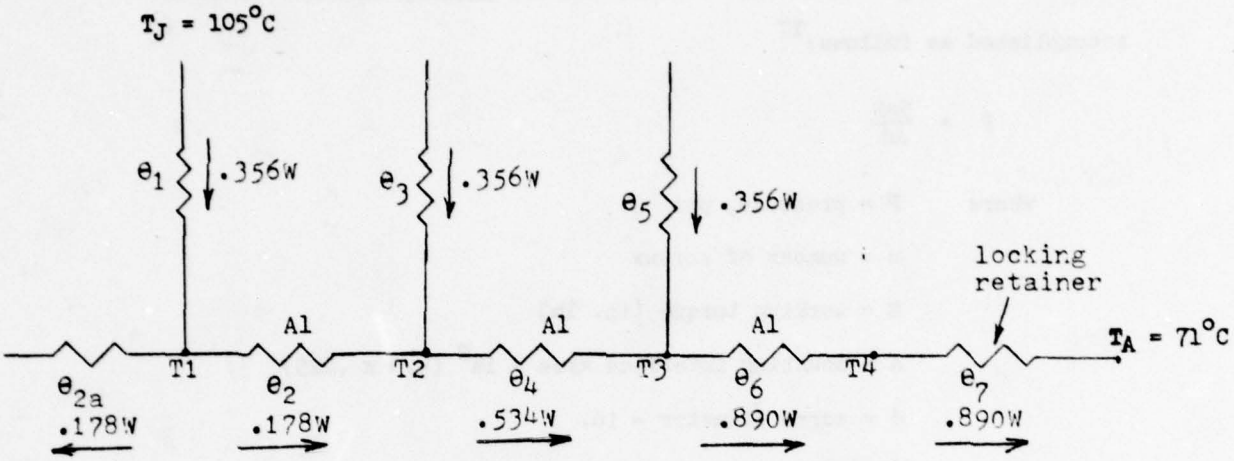
$$\theta_2 = \frac{45.87}{2.61} = 17.57^{\circ}C/\text{watt}$$

$$\theta_4 = \theta_2 = 17.57^{\circ}C/\text{watt}$$

$$\theta_6 = \frac{\frac{1}{2}(.85) + 0.125 \quad (12) \ (3.413)}{2.61}$$

$$\theta_6 = 8.63^{\circ}C/\text{watt}$$

* Factor of 2 from AHAM Heat Sink Application Handbook, page 83 (Reasons 4 & 5).



$$\theta_1 = \theta_3 = \theta_5$$

$$\theta_1 = \theta_{JC} + \theta_{c\text{-}al}$$

$$A_{JC} = 25^{\circ}C/watt$$

$$\theta_{c\text{-}al} = \left(\frac{\rho t}{A} \right) \times 2$$

where

ρ = Resistivity in °C in./watt

(thermal joint compound) = 55°C in./watt

t = thermal coumpound thickness - inches = 0.00/in

A = Area of DIP = (.85 x .25) = 0.212 in^2

FIGURE A-2

Thermal Model

30 - 16 Pin IC Configuration

This makes sense especially with the extensive use of composites anticipated

Solving for Θ_7 using the locking retainer, requires calculation of the pressure existing between the retainer and the housing surface. This is accomplished as follows:[17]

$$P = \frac{5nE}{Ad}$$

where P = pressure, psi

n = number of screws

E = working torque (in. lb)

A = mounting interface area - in^2 (4.0 x .225)

d = screw diameter - in.

$$P = \frac{5(1)(5)}{.9(.06)} = 462 \text{ psi}$$

From curve for screw mounted with no mica insulator:

$$\Theta_7 = .65^\circ C \text{ in}^2/\text{watt}$$

$$\Theta_7 = \frac{.65}{.9} = .722^\circ C/\text{watt}$$

$$\Theta_7 = .722^\circ C/\text{watt (4.0 in)}$$

$$\Theta_7 = 2.89^\circ C \text{ in./watt}$$

For a board height of 4.0 inches with 6 rows:

$$\frac{4.0}{6} = .667 \text{ in./row}$$

$$\Theta_7 = \frac{2.89^\circ C \text{ in}}{.667 \text{ watt in}} = 4.33^\circ C/\text{watt}$$

$$\Delta T = \Theta P$$

$$105 - T1 = \Theta_1 (.356W)$$

$$T1 = 105 - 25.518 (.356)$$

$$T1 = 95.92^\circ C$$

$$T1 - T2 = \Theta_2 (.178W)$$

$$T2 = 95.92 - 17.57 (.178)$$

$$T2 = 92.79^{\circ}C$$

$$T2 - T3 = \Theta_4 (.534W)$$

$$T3 = 92.79 - 17.57 (.534)$$

$$T3 = 83.41^{\circ}C$$

$$T3 - T4 = \Theta_6 (.890W)$$

$$T4 = 83.41 - 8.63 (.890)$$

$$T4 = 75.73^{\circ}C$$

$$T4 - T_A = \Theta_7 (.890W)$$

$$T_A = 75.73 - 4.33 (.890)$$

$$T_A = 71.88^{\circ}C$$

To determine approximate total power dissipation available for module

$$\Delta T = \Theta P1$$

with P1 = power dissipation per IC

$$\Delta T = \Theta_1 P_1 + \Theta_2(.5P1) + \Theta_4(1.5P1) + \Theta_6(2.5P1) + \Theta_7(2.5P1)$$

$$105 - 71 = (25.52 + 8.78 + 26.35 + 21.58 + 10.82) \times P1$$

$$P1 = 0.365 \text{ watt}$$

$$P_{board} = 0.365 \text{ watt} \times 30 \text{ DIPS} = 10.96 \text{ watts}$$

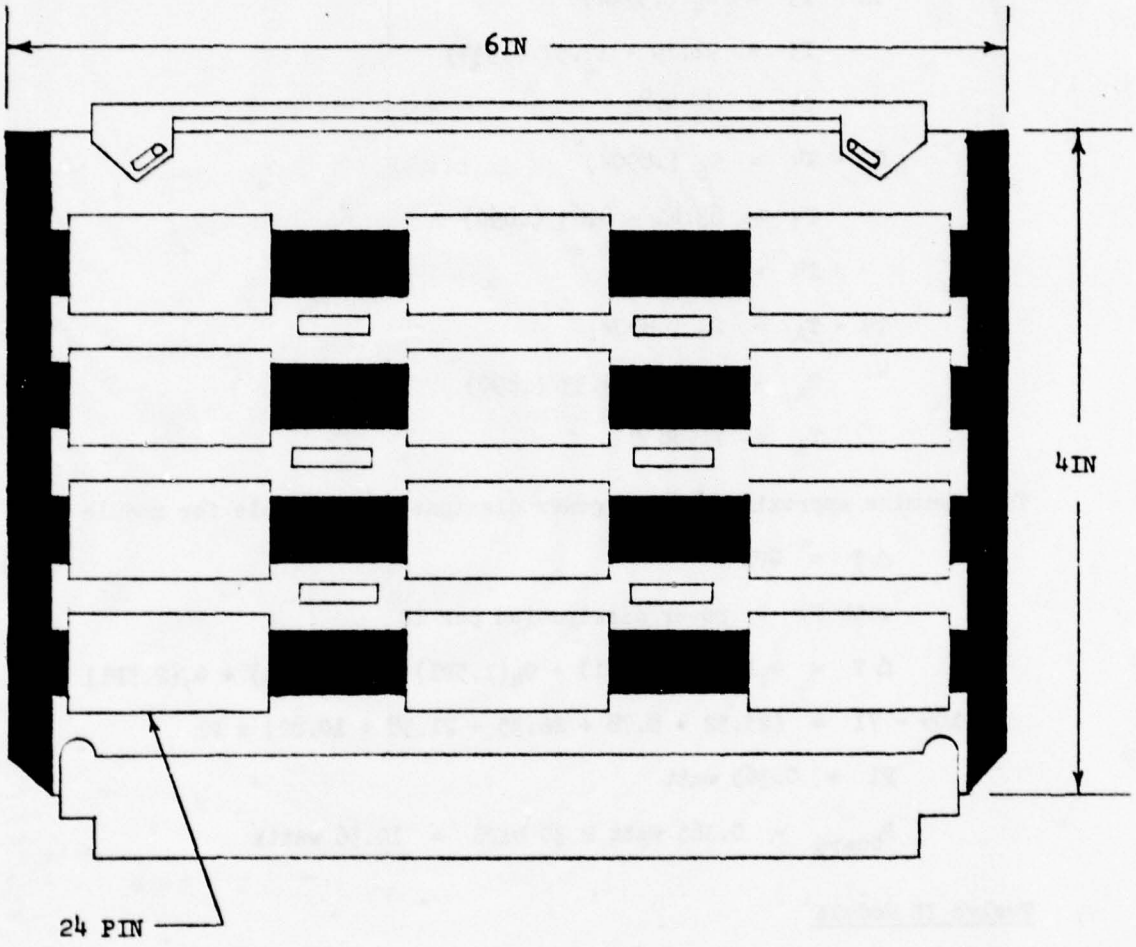
Twelve IC Module

The configuration for mounting 12-24 pin IC's is shown in Figure A-3 with the thermal model shown in Figure A-4.

The aluminum conducting strips for the module are 0.40 inches in width by 0.05 inches in thickness.

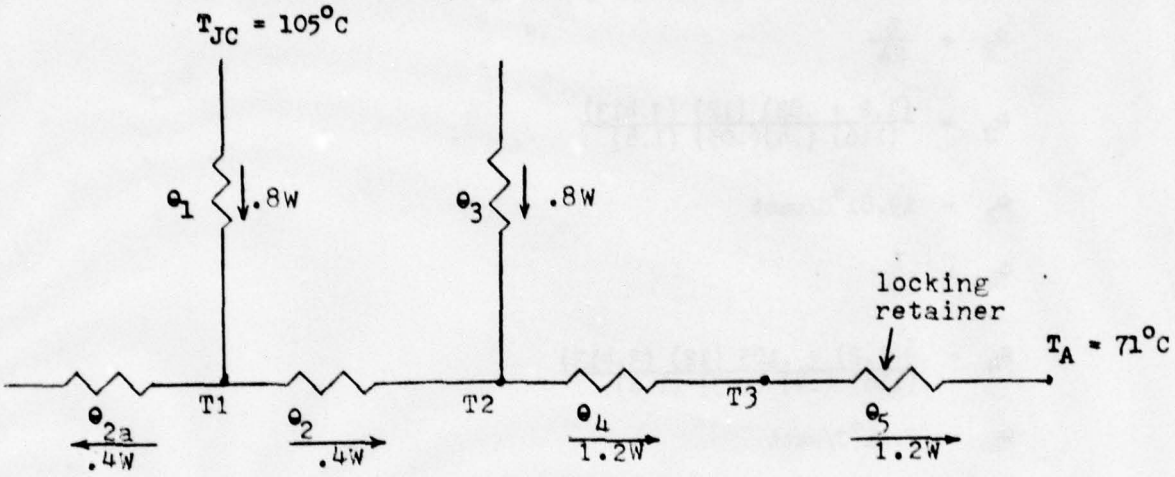
From Table A-1, the total power dissipation required is 9.60 watts.

$$\frac{9.60 \text{ watts}}{12 \text{ DIPS}} = 0.8 \text{ watts/DIP}$$



TWELVE DUAL IN-LINE PACKAGE INSTALLATION
POWER DISSIPATION - 9.6 WATTS

FIGURE A-3



$$\Theta_1 = \Theta_{JC} + \Theta_{c\text{-}al}$$

$$\Theta_{JC} = 7.37^{\circ}C/watt$$

$$\Theta_{c\text{-}al} = \left(\frac{\rho t}{A}\right) \times 2$$

$$\Theta_{c\text{-}al} = \left(\frac{55 \times .001}{.72}\right) \times 2 = .152^{\circ}C/watt$$

$$\Theta_1 = 7.37 + .152 = 7.52^{\circ}C/watt$$

DIP length = 1.2 inches

Space between DIPS = 0.82 inches

Edge distance (DIP to locking retainer) = 0.125 inches

FIGURE A-4

Thermal Model

12 - 24 Pin IC Configuration

Calculations for the heat dissipation capability follow:

$$\Theta_2 = \frac{L}{KA}$$

$$\Theta_2 = \frac{(1.2 + .82)\ (12)\ (3.413)}{(116)\ (.4)(.05)\ (1.8)}$$

$$\Theta_2 = 19.81^{\circ}C/watt$$

$$\Theta_4 = \frac{L}{KA}$$

$$\Theta_4 = \frac{\frac{1}{2}(1.2) + .125\ (12)\ (3.413)}{(116)\ (.4)\ (.05)\ (1.8)}$$

$$\Theta_4 = 7.11^{\circ}C/watt$$

From prior calculations

Θ for locking retainer = $2.89^{\circ}C$ in/watt

$$\frac{\text{Board Width}}{\text{No. of Rows}} = \frac{4.0}{4} = 1.0 \text{ in/row}$$

$$\Theta_5 = \frac{2.89^{\circ}C \text{ in}}{1 \text{ in watt}}$$

$$\Theta_5 = 2.89^{\circ}C/watt$$

$$\Delta T = \Theta P$$

$$105 - T1 = \Theta_1\ (.8W)$$

$$T1 = 105 - 7.52\ (.8)$$

$$T1 = 98.98^{\circ}C$$

$$T1 - T2 = \Theta_2\ (.4W)$$

$$T2 = 98.98 - 19.81\ (.4)$$

$$T2 = 91.06^{\circ}C$$

$$T2 - T3 = \Theta_4\ (1.2W)$$

$$T3 = 91.06 - 7.11\ (1.2)$$

$$T3 = 82.53^{\circ}C$$

$$T3 - T_A = \Theta_5 (1.2W)$$

$$T_A = 82.53 - 2.89 (1.2)$$

$$T_A = 79.06^{\circ}C$$

Total power dissipation available

$$\Delta T = \Theta P$$

$$\Delta T = \Theta_1 P_1 + \Theta_2(.5P1) + \Theta_4(1.5P1) + \Theta_5(1.5P1)$$

$$105 - 71 = (7.52 + 9.90 + 10.66 + 4.33) \times P1$$

$$P1 = 1.05 \text{ watt}$$

$$P_{board} = 1.05 \text{ watt} \times 12 \text{ DIPS} = 12.6 \text{ watts}$$

Six IC Module

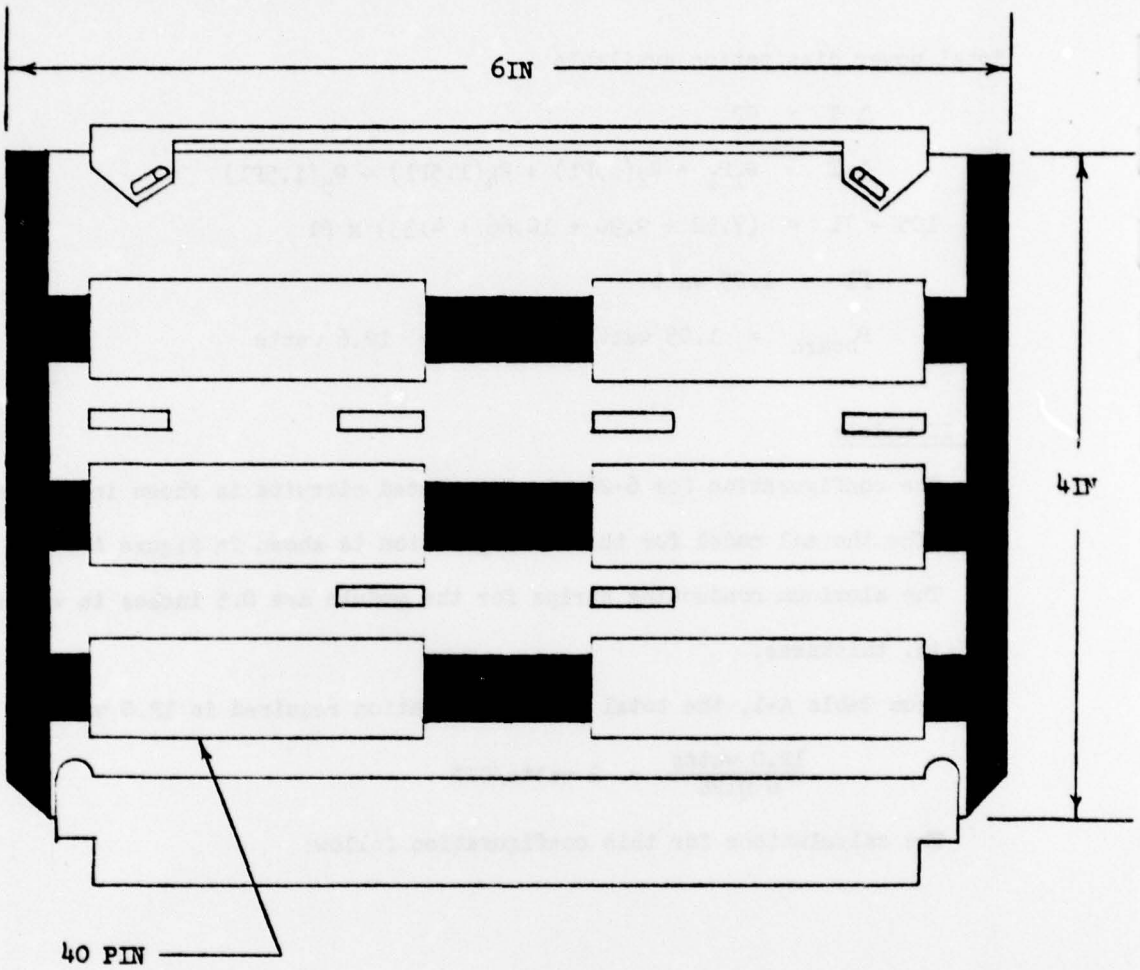
The configuration for 6-24 pin integrated circuits is shown in Figure A-5. The thermal model for this configuration is shown in Figure A-6.

The aluminum conducting strips for the module are 0.5 inches in width by 0.05 in. thickness.

From Table A-1, the total power dissipation required is 12.0 watts

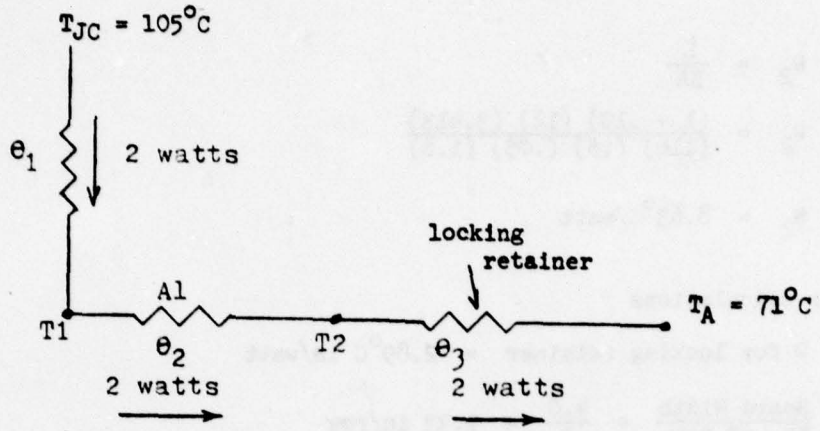
$$\frac{12.0 \text{ watts}}{6 \text{ DIPS}} = 2 \text{ watts/DIP}$$

The calculations for this configuration follow:



SIX DUAL IN-LINE PACKAGE INSTALLATION
POWER DISSIPATION - 12 WATTS

FIGURE A-5



$\theta_1 = \theta_{JC} + \theta_{c\text{-}al}$

$\theta_{JC} = 4.42°C/watt$

$\theta_{c\text{-}al} = \left(\frac{55\ (.001)}{1.2} \right) \times 2 = .0916°C/watt$

$\theta_1 = 4.42 + .092 = 4.512°C/watt$

DIP length = 2 inches

Space between DIPS = 1 inch

Edge distance (DIP to locking retainer) = 0.100 inch

Thermal Model
6 - 40 Pin IC Configuration

FIGURE A-6

$$\Theta_2 = \frac{L}{KA}$$

$$\Theta_2 = \frac{(1 + .10)\ (12)\ (3.413)}{(116)\ (.5)\ (.05)\ (1.8)}$$

$$\Theta_2 = 8.63^{\circ}C/watt$$

From prior calculations

Θ for locking retainer = $2.89^{\circ}C$ in/watt

$$\frac{\text{Board Width}}{\text{No. of Rows}} = \frac{4.0}{3} = 1.33 \text{ in/row}$$

$$\Theta_3 = \frac{2.89^{\circ}C \text{ in}}{1.33 \text{ in watt}}$$

$$\Theta_3 = 2.17^{\circ}C/watt$$

$$\Delta T = \Theta P$$

$$105 - T1 = \Theta_1 (2W)$$

$$T1 = 105 - 4.512\ (2)$$

$$T1 = 95.98^{\circ}C$$

$$T1 - T2 = \Theta_2 (2W)$$

$$T2 = 95.98 - 8.63\ (2)$$

$$T2 = 78.72^{\circ}C$$

$$T2 - T_A = \Theta_3 (2W)$$

$$T_A = 78.72 - 2.17\ (2)$$

$$T_A = 74.38^{\circ}C$$

Total power dissipation available

$$\Delta T = \Theta P$$

$$\Delta T = \Theta_1 P_1 + \Theta_2 P1 + \Theta_3 P1$$

$$105 - 71 = (4.51 + 8.63 + 2.17) \times P1$$

$$P1 = 2.22 \text{ watts}$$

$$P_{board} = 2.22 \text{ watts} \times 6 \text{ DIPS} = 13.35 \text{ watts}$$

Birtcher Clip Thermal Analysis

The following calculations are presented to indicate the advantage in using the locking retainers in place of the Birtcher clips for sidewall heat transfer. Only the power dissipation capability based upon 30 DIPS installed on 6 inch by 4 inch glass epoxy board with aluminum strips and Birtcher clips to transfer heat from the module components to the sidewall will be calculated since, from Table A-1, the power dissipation capabiltiy using locking retainers has been determined to be 10.96 watts.

From prior calculations for 30 DIP module:

$\theta_1 = 25.518^\circ C/watt$ $\theta_2 = 17.57^\circ C/watt$

$\theta_4 = 17.57^\circ C/watt$ $\theta_6 = 8.63^\circ C/watt$

Solving for θ_7: Birtcher clip resistance

The Birtcher clip thermal resistance is $11.1^\circ C$ in./watt from the IBM report.[9]

$$\frac{\text{Board Width}}{\text{No. of Rows}} = \frac{4.0 \text{ in.}}{6} = 0.667 \text{ in./row}$$

$$\theta_7 = \frac{11.1^\circ C \text{ in.}}{.667 \text{ watt in.}} = 16.64^\circ C/watt$$

$$\Delta T = \theta P$$

$$105 - 71 = \theta_1(P1) + \theta_2(.5P1) + \theta_4(1.5P1) + \theta_6(2.5P1) + \theta_7(2.5P1)$$

$$34 = (25.518 + 8.78 + 26.35 + 21.57 + 41.6)\ P1$$

$$P1 = .274 \text{ watt}$$

$$P_{board} = .274 \text{ watt} \times 30 \text{ DIPS} = 8.24 \text{ watts}$$

This is a reduction of approximately 25% in power handling capability for the module and does not provide the required Power Dissipation capability of 10.68 watts.

The aluminum strip width of 0.25 is considered acceptable for the following reasons: The pin spacing on DIPS is 0.30 in. The hole size for the pin leads is 0.025 in. diameter. This would leave 0.012 inches between the edge of the hole and the aluminum strip. In addition, the aluminum strips will be anodized, making them non-conductive.

APPENDIX B

THERMAL AND VIBRATION ANALYSIS

CHIP CARRIER CONFIGURATION

Chip Carrier Installation

Conclusions reached in the General Electric Company Report "Modular Avionics Packaging (MAP)"[18], are that chip carriers (cc) will replace dual in-line packages (DIPS) as the packaging standard by 1985. Figure B-1 illustrates the proposed 6 inch by 4 inch module with 30, 16 pin chip carriers mounted on a ceramic substrate and attached to an aluminum frame. Interconnection to the module is accomplished through a standard two-row, 100 pin connector. The 100 pin connector effectively pin limits the quantity of chip carriers to approximately 30 IC's of 18 gates each for a total of 540 gates. The aluminum frame is used for conduction cooling of the chip carriers to the sidewall thru locking retainers. Power dissipation capability for this configuration is 14.47 watts. For a minimum board height of 2 inches, the power dissipation capability for the 30 chip carriers is 11.43 watts. Figure B-2, presents the power dissipation capability of this type of module as a function of module height. Thermal calculations for the 6 inch by 4 inch module are presented below for the thermal model of Figure B-3.

These calculations are based upon the use of a ceramic substrate for mounting of the chip carrier. There are other possible technologies available for this purpose such as porcelanized steel, polyimide board, etc.. These construction methods may also be applicable to the use of DIP's and flatpacks. These various techniques have not been analyzed herein since each is a different situation. Mounting of chip carriers on ceramic appears to be the presently accepted method and is presented for information.

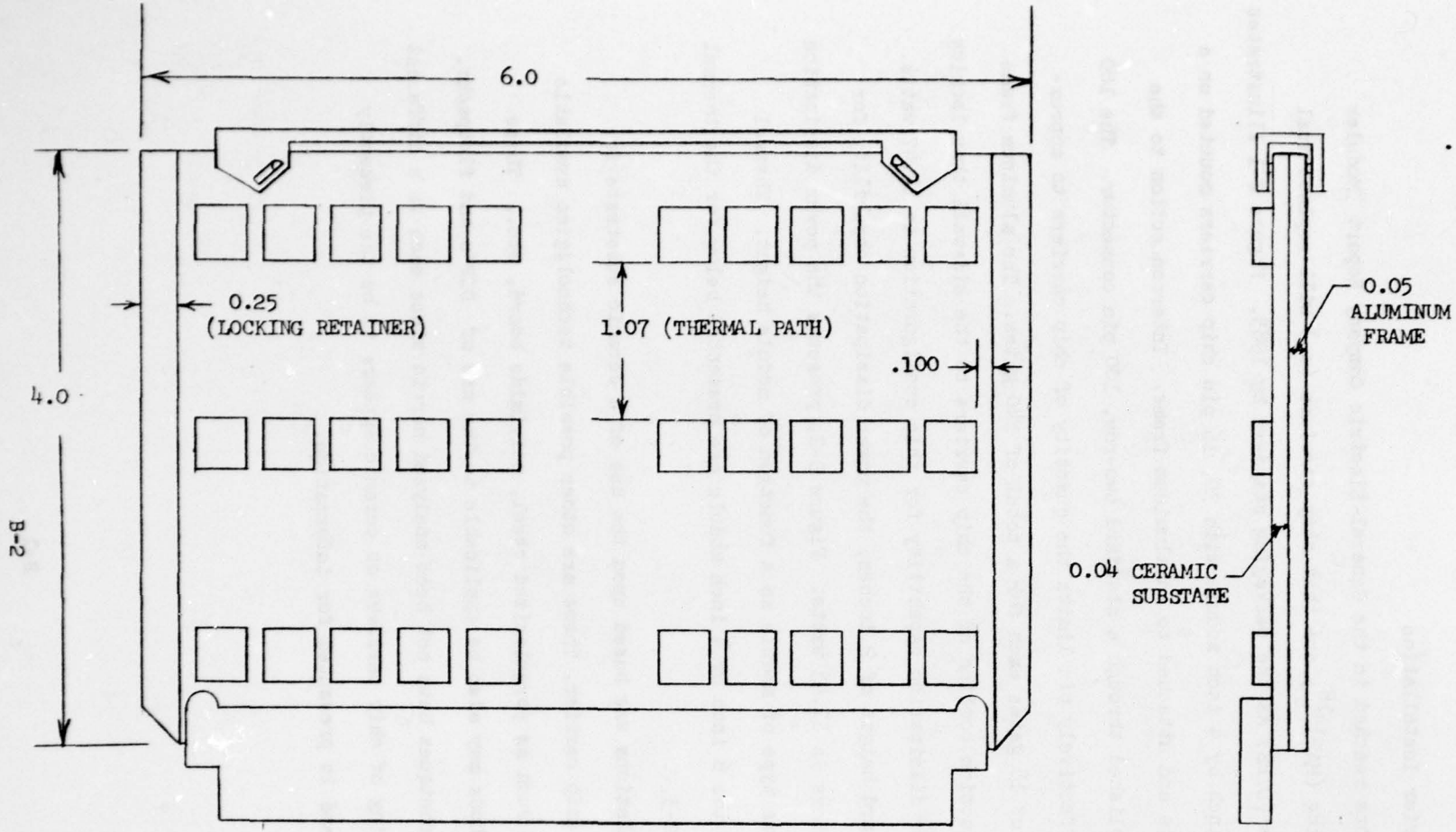
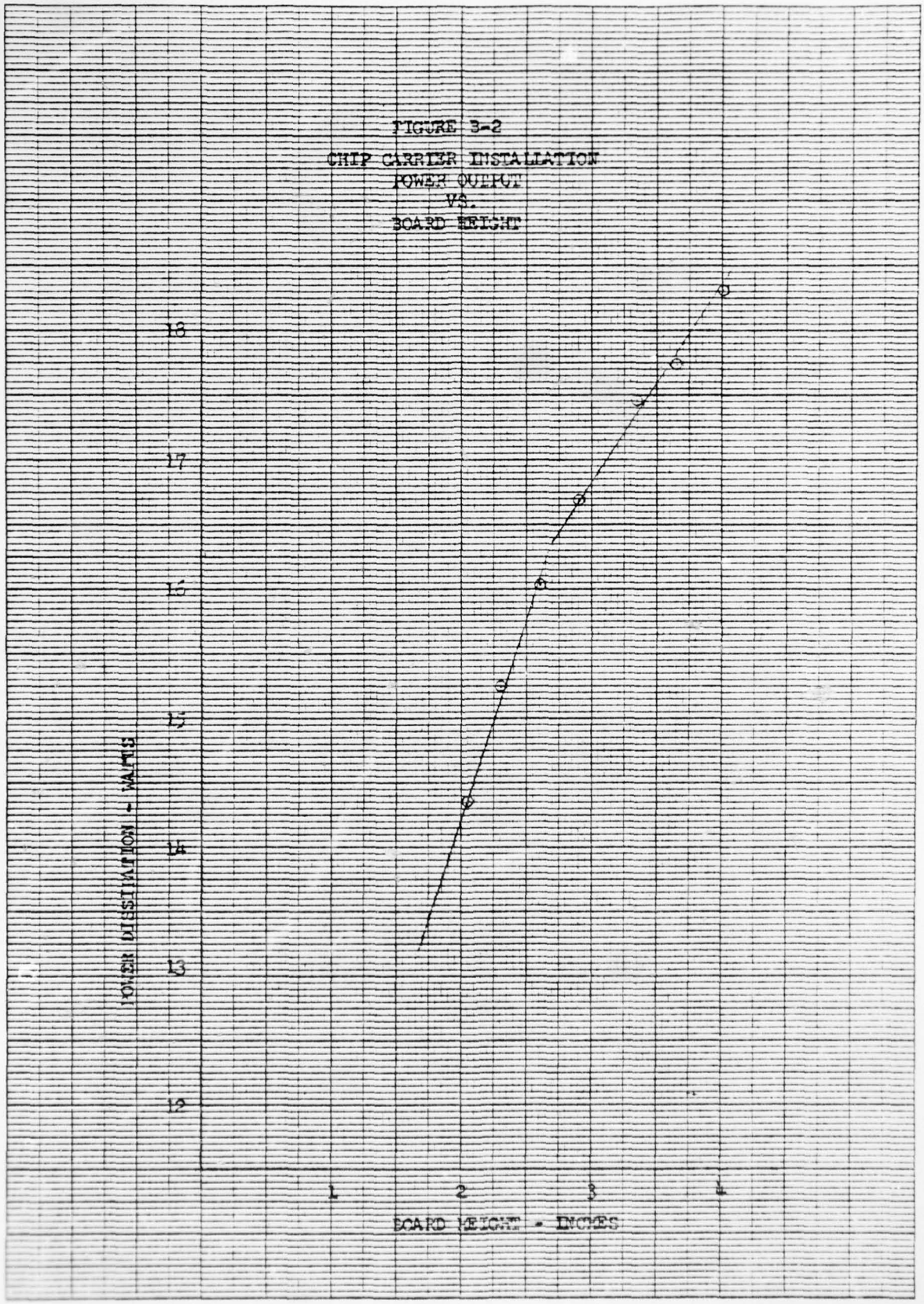
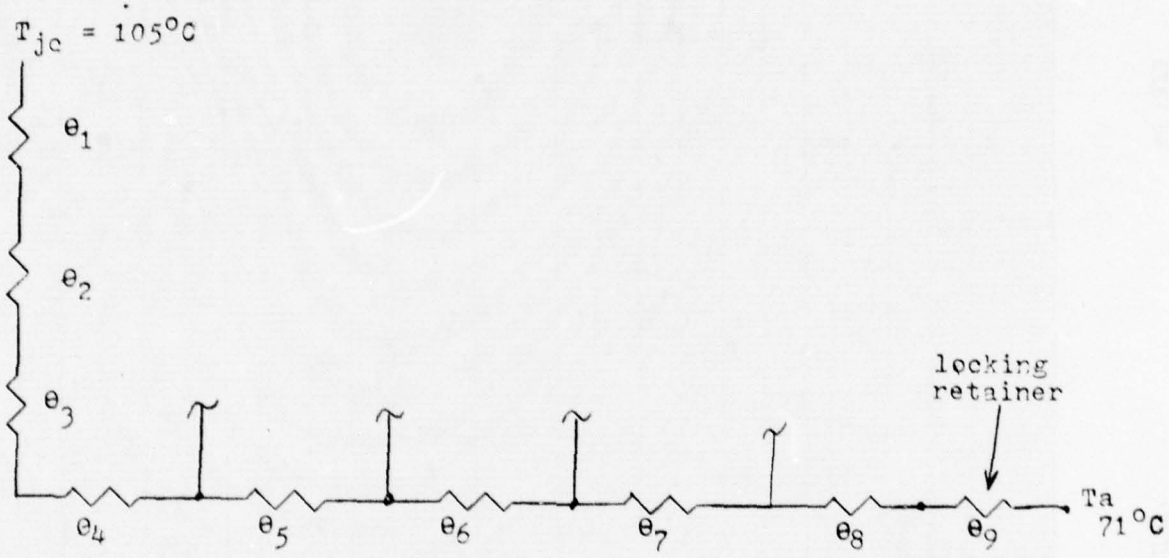


FIGURE B-1 . CHIP CARRIER INSTALLATION



46 1323

K&E 10 X 10 TO ½ INCH 7 X 10 INCHES
KEUFFEL & ESSER CO MADE IN U.S.A.



Thermal Model

30 Chip Carrier IC Configuration

Figure B-3

The following calculations are based upon $\frac{1}{2}$ of 1 row with dissipation of the other $\frac{1}{2}$ of the row assumed to be equal in magnitude.

Using thermal transfer characteristics of the chip carrier[18] and a thermal path width of 1.07 in.

θ_1 = 30° C/watt (junction to case)

θ_2 = 7.42° C/watt (case to ceramic substrate)

θ_2 calculated using conductivity value of 0.0044 watt/ in.° C[18] which is equal to $\frac{1}{\rho}$

$$\theta_2 = \frac{\rho t}{A}$$

where t is the thickness in inches (.004)

A = chip carrier surface area = $(.35^2)$

$$\rho = \frac{1}{.0044} = 227.27^\circ \text{ C in./watt}$$

$$\theta_2 = \frac{227.27\ (.004)}{.35^2} = 7.42^\circ \text{ C/watt}$$

θ_3 = .695° C/watt (through substrate)

θ_3 was calculated using the alumina ceramic conductivity value[18] of 0.469 watt/ in.°C

$$\theta_3 = \frac{\rho t}{A}$$

$$\rho = \frac{1}{.469} = 2.13^\circ \text{ C in./watt}$$

$$\theta_3 = \frac{2.13\ (.04)}{.35^2} = .695^\circ \text{ C/watt}$$

$$\theta_4 = \frac{L}{KA}$$

$$\theta_4 = \frac{(.35 + .1)\ (12)\ (3.413)\ \text{BTU/watt hr } ^\circ\text{C in.}}{(116\ \text{BTU/ft hr } ^\circ\text{F})\ (1.07\ \text{in})\ (.05\ \text{in})\ (1.8^\circ\text{F})}$$

$$\theta_4 = 1.65^\circ\text{C/watt} = \theta_5 = \theta_6 = \theta_7$$

$$\theta_8 = \frac{(.175 + .100)\ (12)\ (3.413)}{(116)\ (1.07)\ (.05)\ (1.8)}$$

$$\theta_8 = 1.01^\circ\text{C/watt}$$

From prior calculations on the locking retainer

$$\theta_9 = .722^\circ\text{C/watt} \times 4.0\ \text{in (Board Height)}$$

$$\theta_9 = 2.888^\circ\text{C in/watt}$$

$$\frac{\text{Board Height}}{\text{No. of Rows}} = \frac{4.0\ \text{in}}{3} = 1.33\ \text{in/row}$$

$$\theta_9 = \frac{2.888^\circ\text{C in}}{1.33\ \text{in watt}}$$

$$\theta_9 = 2.17^\circ\text{C/watt}$$

$$\Delta T = \theta P$$

$$105 - 71 = \theta_1 P + \theta_2 P + \theta_3 P + \theta_4 P + \theta_5(2P) + \theta_6(3P) + \theta_7(4P) + \theta_8(5P) + \theta_9(5P)$$

$$34 = (30 + 7.42 + .695 + 1.65 + 3.3 + 4.95 + 6.6 + 5.05 + 10.85) \times P$$

$$P = .482\ \text{watt}$$

$$P_{board} = .482\ \text{watt} \times 30\ \text{CC} = 14.47\ \text{watts max}$$

This represents a power dissipation capability increase of approximately 3.5 watts from the glass epoxy board with DIP's and aluminum conducting strips.

Calculations for other board heights are performed in identical fashion with the exception of the thermal path width and resistance calculations for the reduced size of the locking retainer.

With the combination of the alumina ceramic substrate and aluminum frame, the fundamental resonant frequency of the 6 inch by 4 inch board is 717 Hz. This is an increase in resonant frequency over the glass epoxy board with aluminum strips due to the increase of the board bending stiffness factor, D. This stiffness factor is calculated using the modulus of elasticity of the alumina ceramic-aluminum frame, which is greater than the glass epoxy-aluminum strip combination. The fundamental resonant frequency of the glass epoxy-aluminum strip combination was in the range of 386 to 564 Hz, depending upon exact component layout.

The alumina ceramic substrate and aluminum frame, therefore, provides a significant improvement in the thermal characteristics and a slight improvement in the vibration characteristics of the module over the glass epoxy/aluminum conducting strip configuration.